Fermi National Accelerator Laboratory

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SMQIE: The Shower Max QIE Chip

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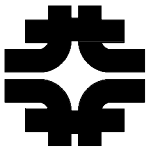

SMQIE: The Shower Max QIE Chip

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1 Abstract

A QIE-like full-custom chip has been designed by members of the Fermilab PPD/ETT/ES Group as well as members of the CDF/Shower Max Group. This chip contains two channels each with an eight range QIE front end capable of handling charges from roughly 12 fC to roughly 100 pC. Each channel also contains a five-bit flash A-to-D converter, a 38 stage deep FIFO for level 1 trigger delay and storage for holding selected time slices. It communicates with the outside world via LVDS-like differential signals.

This chip utilizes a 1.2μm double-metal, double-polysilicon process with a vertical NPN transistor option. It has been prototyped using ORBIT Semiconductor's Foresight program. As of this writing, it has been submitted to Super Tex (new owner of the ORBIT fabrication facility) for fabrication. However, it has not yet returned from fabrication.

2 Introduction

QIE stands for Charge Integrator and Encoder. This family of chips provides logarithmic analog to digital conversion. They sample a charge, select and encode an appropriate range for that charge and provide an offset voltage appropriate to that charge and range. The SMQIE, short for Shower Max QIE, was intended from the beginning to be a "complete solution" to the logarithmic analog to digital conversion problem. Furthermore, it was to be a "well behaved" QIE. "Complete solution" means that it would contain an internal flash analog to digital converter to translate the voltage offset into a digital mantissa value that could be dealt with directly by DAQ systems. It would also contain a Level 1 delay FIFO as well as appropriate circuitry to either select or eliminate a given time slice depending on the presence or absence of a Level 1 Trigger. Finally, it would contain buffers to hold

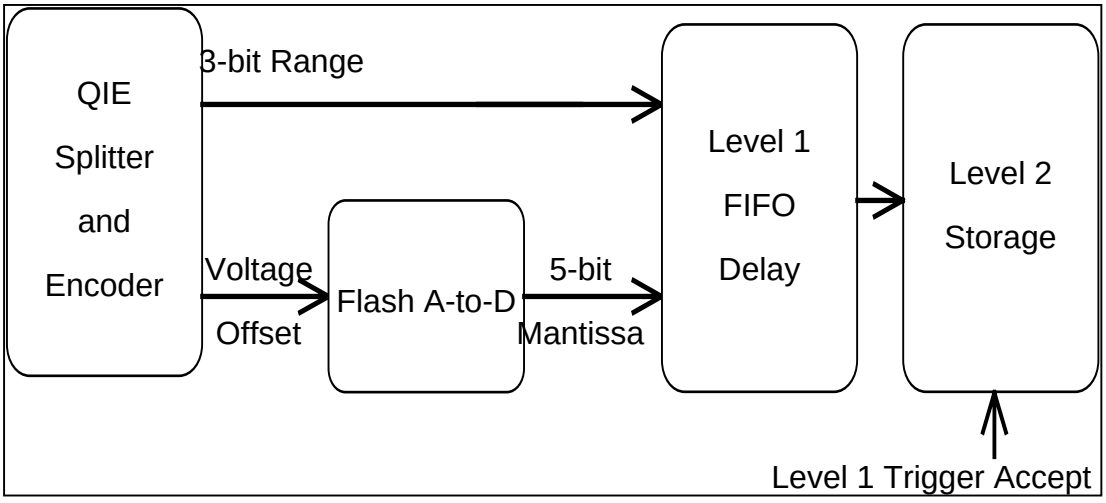

Figure 1 : General flow diagram of the SMQIE

selected range/mantissa pairs until the DAQ system could retrieve them. "Well behaved" simply means that the SMQIE would operate on zero to 5-volt power rails and would not require the PC board to provide exotic voltages in order to operate properly. Figure 1 shows the general flow chart of the SMQIE chip.

In addition to these general requirements, the Shower Max has a number of specific requirements for the experiment[1]. These are given in the following table.

Table 1 : Shower Max Requirements

Full Scale Input Charge	100 pC
Number of Ranges	8
Flash Resolution	5-bit
LSB Resolution on I/2 Range	12.5 fC
Overall Precision	12.5 fC or 3% (whichever is greater)
Input Frequency	7.6 MHz (1/132 ns)
Output Voltage Levels	LVDS standard

Shower Max detector system can be divided into two logical pieces: the Plug and the Central. The majority of the Shower Max channels will be dedicated to the Central, which

[1] "Specifications for the Shower Max QIE" by G. Drake April 30, 1997 available at "http://www-cdf.fnal.gov/runII_spec/spec_smqie.txt"

is comprised of relatively slow strip chambers. Signals in the Central will require four 132ns time slices to output all of the charge from a single event. The Plug, on the other hand, is made of relatively fast photomultiplier tubes, which will output all of the charge from a single event within one 132ns time slice. The SMQIE must be capable of servicing both the Plug and the Central.

Finally, the Shower Max project will process the outputs of approximately 17,600 channels. At two channels per chip, there must be 8,800 working SMQIE chips. The project requires them to be bonded into thin quad flat packs (TQFPs). A yield of 60% was assumed based on previous experience with similar chips like the KteV QIE. This yield means that 14667 chips must be fabricated to meet our minimum requirements. A single wafer can hold 256 SMQIE chips and wafers are processed in lots of 20 wafers. Therefore, three lots of 20 wafers each (15360 chips) will be requested of the manufacturer.

3 The Front End

3.1 The Splitter

The basic operation of the Splitter is very straightforward. A current pulse at the emitters of an array of bipolar transistors will split itself among the bipolar transistors. By grouping the bipolar transistors in a binary arrangement as show in Figure 2, a binary splitting of the current can be expected. It is not necessary to use bipolar transistors. MOS transistors can also be used, but the split ratios are not usually as good due to threshold voltage mismatch and other process variations. In fact, early versions of the SMQIE used MOS transistors,

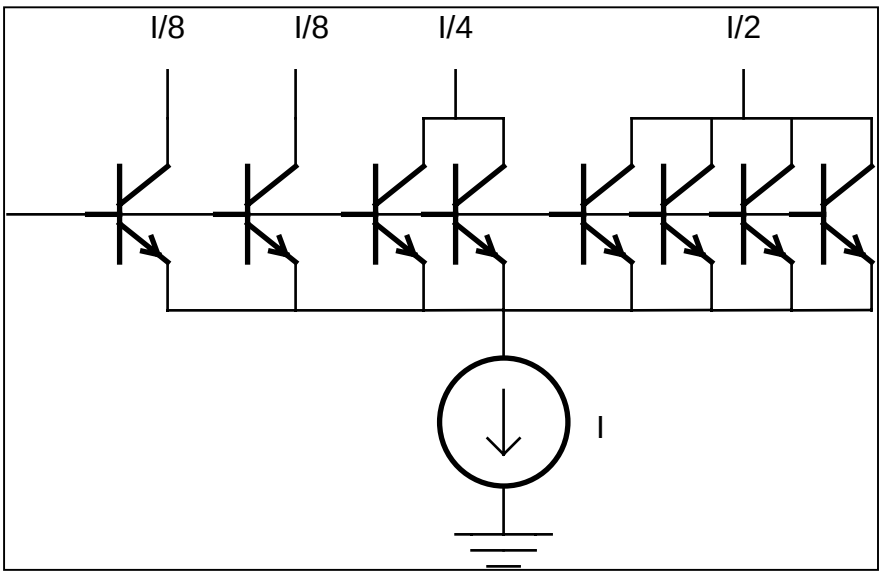

Figure 2 : Basic Splitter function

but these were replaced by bipolar transistors when they became available in the 1.2μm process. To achieve the eight ranges necessary for the Shower Max project, an array of 128 bipolar transistors were used divided into groups of 64, 32, 16, 8, 4, 2, 1 and 1. To achieve eight unique ranges from seven unique currents (one repeated twice), Range 7 is integrated onto a capacitor twice the size of the other capacitors.

3.2 Splitter Feedback Amplifier

In reality, it is not sufficient to have a splitter as shown in Figure 2. First, the impedance as seen from the emitter of a bipolar transistor is inversely proportional to the emitter current. At very low currents, therefore, the input impedance of the circuit in Figure 2 can become very large. Since there will be a capacitance associated with the cable which connects to the input of the SMQIE, there will be an unacceptably large RC charging delay every time

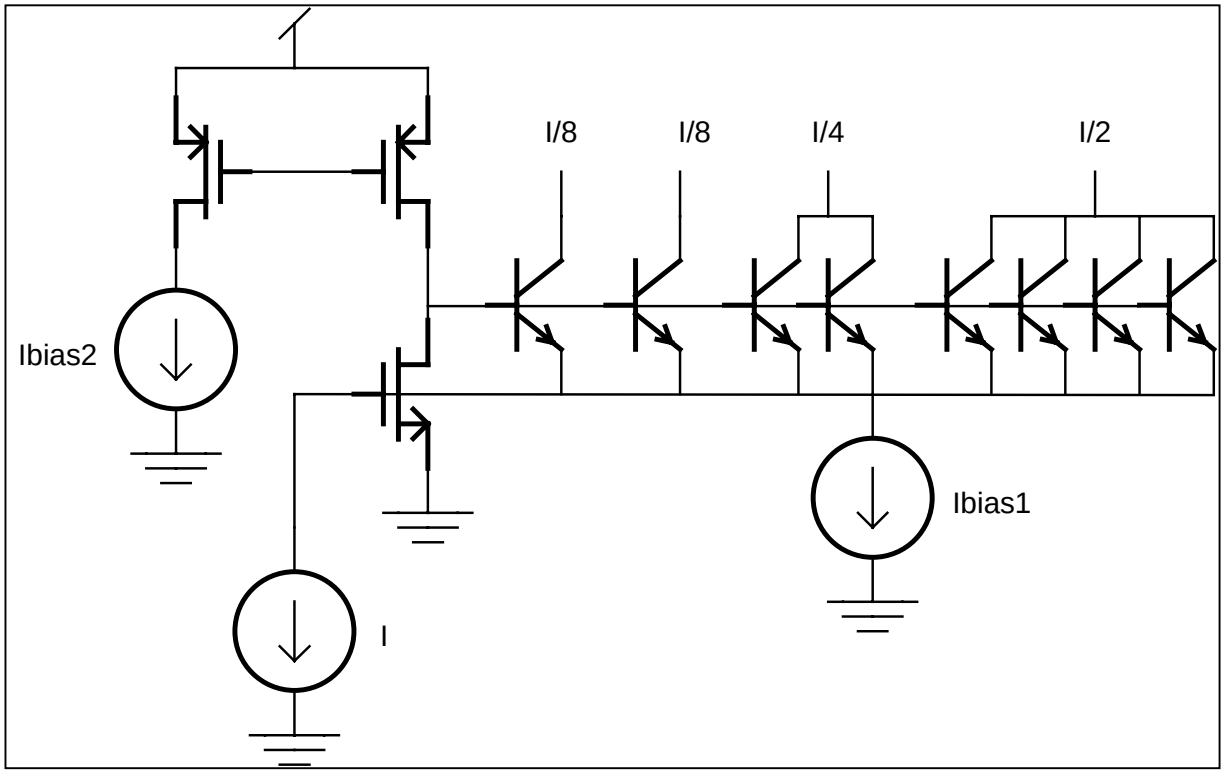

Figure 3 : Splitter with Feedback Amplifier

any pulse arrives. Therefore, a DC bias current is necessary to reduce the input impedance of the splitter during small pulses and quiescent operation.

Moreover, in order to keep the input (emitter) voltage constant and to further reduce the input impedance, it is necessary to use a feedback amplifier. This is shown in Figure 3. Since the Shower Max uses the Beam Crossing Clock (7.6 MHz) a simple inverting amplifier with a gain of approximately 50 is sufficient to the task. Note: this Splitter-Feedback configuration forces the user to provide two bias currents, the **Splitter Bias** shown in the figure as Ibias1 and the **Feedback Bias** shown in the figure as Ibias2.

3.3 Cascode

Theoretically, once the input current has been split into the different ranges, it would be possible to integrate the split currents onto eight capacitors similar to the figure below. The

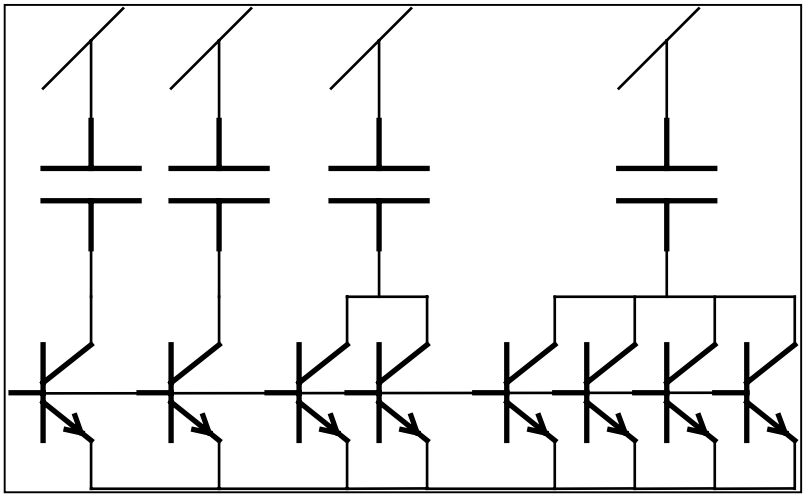

Figure 4 : Simple Splitter with Integrating Capacitors

sum of the voltage across each of these eight capacitors times their capacitance would be equal to the charge that has passed through the input of the splitter. However, reality is not so forgiving. Even current splitting depends on a relatively constant collector voltage. This is even more critical in the case of MOS transistor splitters. Therefore, additional circuitry is necessary to isolate the collector voltage from any voltage changes occurring upstream (such as in the integrating capacitors). This additional circuitry takes the form of a cascode transistor between the splitter collectors and the voltage changes taking place upstream. This is shown in the figure below. As long as the cascode transistors are in saturation and as long as the Splitter Bias current is large by comparison to the input current, then the collector voltage will be largely isolated from the effects of the integrating capacitors.

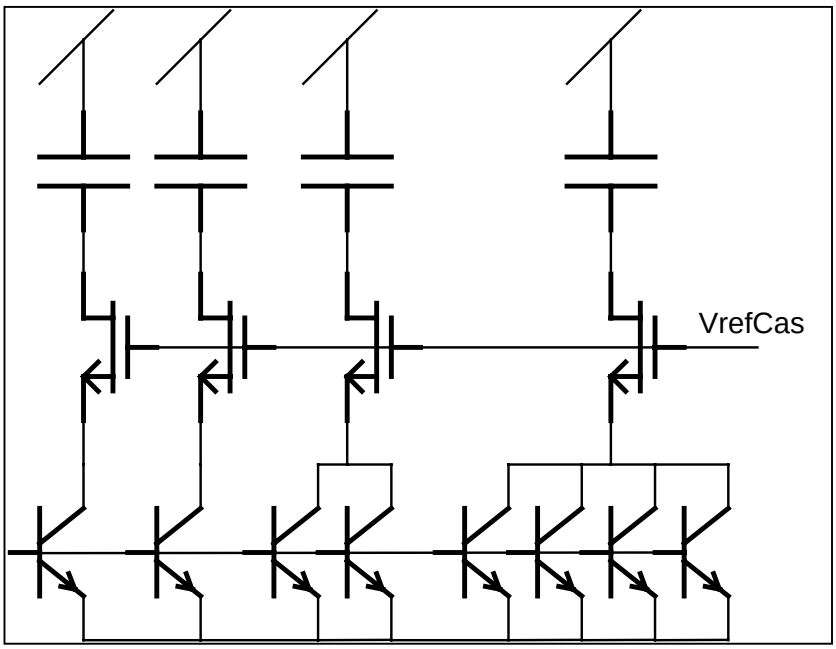

Figure 6 : Splitter with Simple Cascode and Integrating Capacitors

However, in making this modification, another problem has been introduced, and that is that the parasitic capacitances of the collectors of the splitter. These capacitances can get quite large, especially in the I/2 range where there are 64 collectors in parallel (see Figure below). The cascode transistor isolates the collectors from the voltage changes upstream,

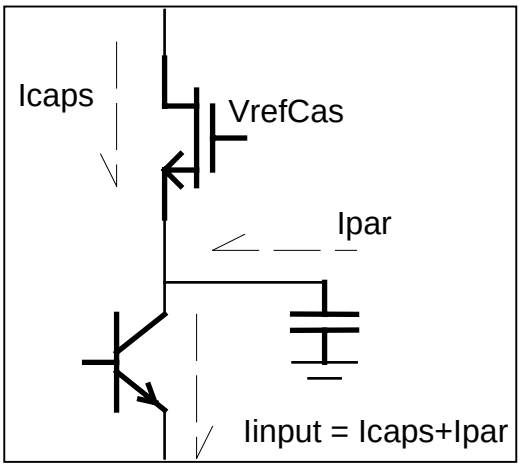

Figure 7: Parasitic Collector Capacitance Effect

but not perfectly. There are small voltage changes at the collectors, and these small voltage changes result in a charge loss to the integrating capacitors as the current from the parasitic capacitors adds to the current from the integrating capacitors to equal the required input current. This charge loss will eventually be regained, of course, when the collector voltages return to their quiescent values and the current from the parasitic capacitors reverses its direction. However, this may not happen fast enough. Therefore, a more sophisticated cascode arrangement, called the regulated cascode, is necessary to make sure the collector voltage moves as little as possible. In this configuration, shown in Figure 8, transistor M1

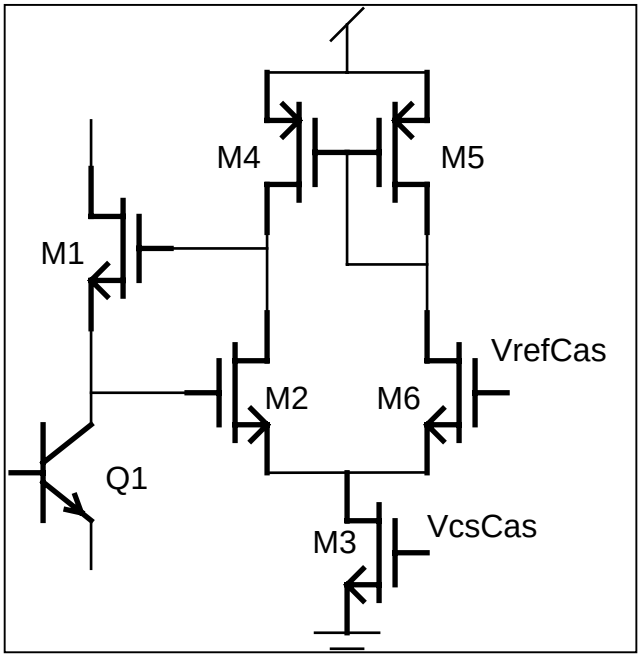

Figure 8: The Regulated Cascode

is the cascode transistor, and transistors M2 and M4 work together as an inverting amplifier such that whenever the collector of the bipolar Q1 moves up or down, the gate voltage of M1 is adjusted to compensate. M3, M5 and M6 work together with M2 and M4 as a

differential amplifier. In this configuration, the collector of Q1 is held to a voltage equal to VrefCas. There are two minor problems to this scheme:

1. One of these regulated cascode amplifiers is necessary for each range. Moreover, each range will require a Cascode circuit of a different size. The cascode transistor (M1 in Figure 8) needs to be scaled for each range so that it can handle the scaled currents of that range. The input transistors of the feedback amplifier (M2 and M6 in Figure 8) need to be scaled for each range to balance the parasitic capacitance in each range. The current source transistor (M3 in Figure 8) must also be scaled for each range so that the open-loop gains of the feedback amplifiers are the same in all ranges for the same VcsCas. Finally, the active load transistors (M4 and M5 in Figure 8) must be scaled with each range so that the DC operating point remains the same for all ranges.

2. Two additional bias voltages must be supplied, VrefCas, the Cascode reference voltage, and VcsCas, the Cascode amplifier current source input.

On the other hand, it is inherent to differential amplifiers with feedback that they will try to keep the gates of their input transistors (in this case M2 and M6) equal in voltage. Therefore, this scheme is inherently immune to process variation. In other words, we are not relying on a process dependent variable like a threshold voltage to keep the collector voltage equal to VrefCas. This is accomplished through the inherent functionality of a differential amplifier in a negative feedback configuration.

Therefore, with the regulated cascode, the collector voltage of the splitter is held at a known voltage and it is effectively isolated from voltage changes upstream. Simulation and subsequent experimentation suggest that the optimal voltage for VrefCas is 2.0 volts.

3.4 Switch Circuit

The SMQIE is intended to operate at the BCO clock frequency of 7.6 MHz with no dead time. The preceding figures which show integrating capacitors are inadequate to this task

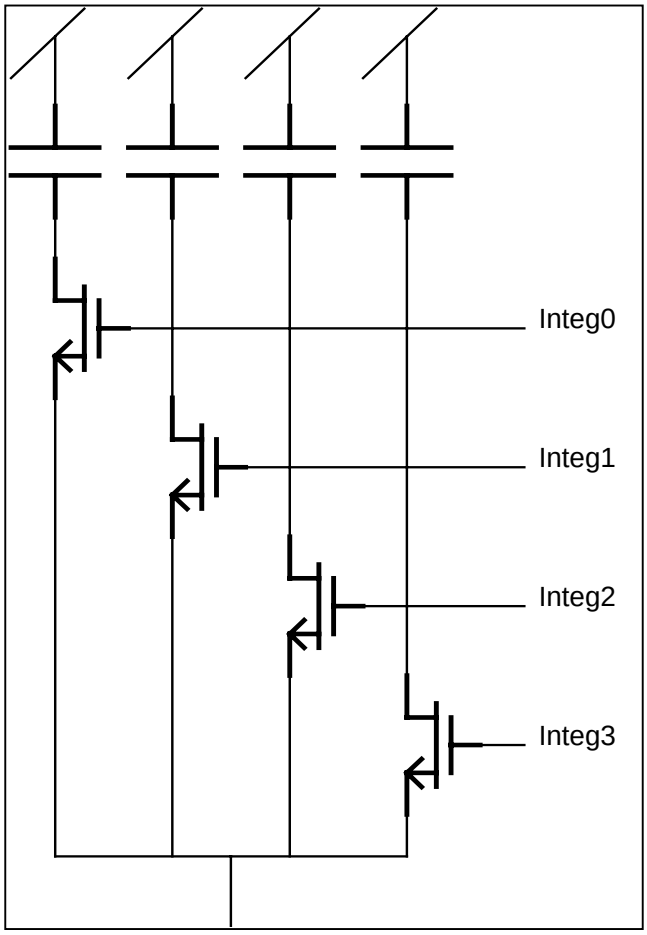

Figure 9 : Simple four-phase analog multiplexer

since a single capacitor cannot simultaneously integrate a charge in the current time slice while it is outputting the voltage result of the previous time slice. Naturally, the system requires more than one integrating capacitor per range and the ability to multiplex between them. In fact, four integrating capacitors are needed per range because of what must happen over an events cycle. First, the capacitor must be reset so that the initial voltage across it is known. Second, the capacitor must be allowed to integrate for the full time slice. Third, some kind of evaluation of the eight (one per range) capacitor voltage values must be made. Finally, the appropriate capacitor voltage value must be output. The details of the evaluation and the outputting will be made clearer in subsequent sections. For now, it is sufficient to indicate that four capacitors per range are necessary so that in any given time slice, one can be resetting, one can be integrating, one can be in the evaluation phase and one can be in the output phase. The Switch Circuit is that part of each range that provides for the multiplexing of the integration phase. The most obvious version of this circuit, the simple analog multiplexer, is shown above.

This simple analog multiplexer has problems because of the parasitic capacitance inherent to the drains of the cascode circuit, which feed its input. As charge is integrated onto, for instance, the Phase0 capacitor (controlled by Integ0), the voltage across the capacitor changes. The voltage at the sources of the transistors of the analog multiplexer will also change, meaning that the parasitic capacitance at the drains of the cascode will be charge to a certain level. In the next time slice, the Phase1 capacitor (controlled by Integ1) must supply current to charge the parasitic cascode capacitance to a new equilibrium level. This new level depends not only on the relative capacitance of the integrating capacitor and the

parasitic cascode capacitor, but also on the voltage integrated in the previous time slice. In short, the simple analog multiplexer "remembers" the previous time slice. One solution to this problem is to recast the cascode feedback amplifier in a slightly different form and use that new form for the switch circuit. This is shown in Figure 10.

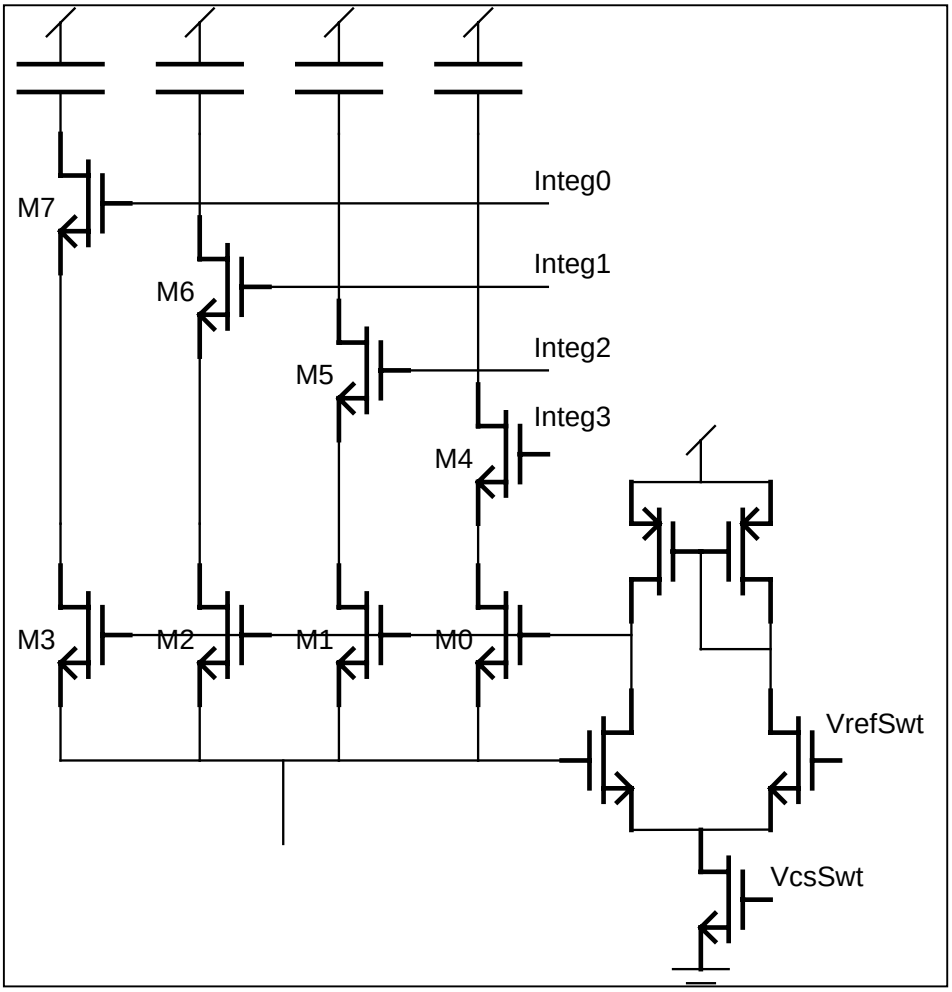

Figure 10: The Switch Circuit with a Regulated Cascode Feedback Amp

Recall that the cascode feedback amplifier stabilized the input voltage at the cascode reference voltage (VrefCas) by using a differential amplifier in a negative feedback configuration. In the case of the cascode feedback amp, the input voltage was the collector of the splitter transistors. In the case of the switch circuit, the input voltage will be the drain of the cascode circuit. There are a number of requirements on the new switch reference voltage (VrefSwt). It must be kept high enough such that the cascode circuit remains alive. In other words, the drain to source voltage across the cascode transistor (M1 in Figure 8) must be large enough that the currents expected to flow in this chip can pass through it (M1). At the same time, VrefSwt must be kept low enough that the cascode and switch transistors (M0 and M4 or M1 and M5 or M2 and M6 or M3 and M7 in Figure 10) in the Switch Circuit are kept alive. Simulations and subsequent experimentation suggested 2.5 volts as the appropriate value for VrefSwt.

It could be said of the Switch Circuit in Figure 10 that it has the same problem with the charging and discharging of parasitic capacitances as the simple analog multiplexer. The only difference is that the problem has been moved from the drains of the Cascode circuit to the drains of M0, M1, M2, or M3 in Figure 10. Technically, this is true. However, the capacitance of the drains of the Cascode circuit can be very large, especially for the I/2 range where the cascode transistor has been scaled to handle the potentially large currents of this range. The Switch Circuit is not scaled with range since it provides direct access to the integrating capacitors. Therefore, it is most important to minimize parasitic capacitance so as much charge as possible will be integrated onto the real capacitor. Consequently, the

parasitic capacitance at the drains of M0, M1, M2 and M3 in Figure 10 is much, much smaller than the parasitic capacitances of the drains of the Cascode circuit.

One final note, it was stated previously that in order to achieve eight unique ranges, it was necessary to integrate Range 7 onto a capacitor that was twice the size of the other capacitors. This is actually achieved in the SMQIE by integrating the Range 7 current onto two parallel capacitors that are identical in every way to the capacitors of the other ranges. This is accomplished through a Switch Circuit with eight outputs (the Switch Circuit in Figure 10 has four outputs). The signals Integ0, Integ1, Integ2 and Integ3 are each connected to two switching transistors. This effectively splits the input current to two parallel capacitors.

3.5 The Dump Circuits

It is obvious from looking at Figure 10 that a large enough charge integrated on any of the capacitors will, eventually, destabilize the Switch Circuit and that the input voltage will begin to drop. An even larger charge will begin to effect the performance of the Cascode circuit as well, and, ultimately, the Splitter. Obviously, such charges should be too large to be interesting. Nevertheless, they can cause problems in subsequent time slices since it will take time for the Splitter, the Cascode and the Switch to recover from such a large charge, and during that time, no reliable data could be taken. Therefore, since such large charges are inevitable, another circuit is necessary to dump excess charge from the Front End and speed its recovery.

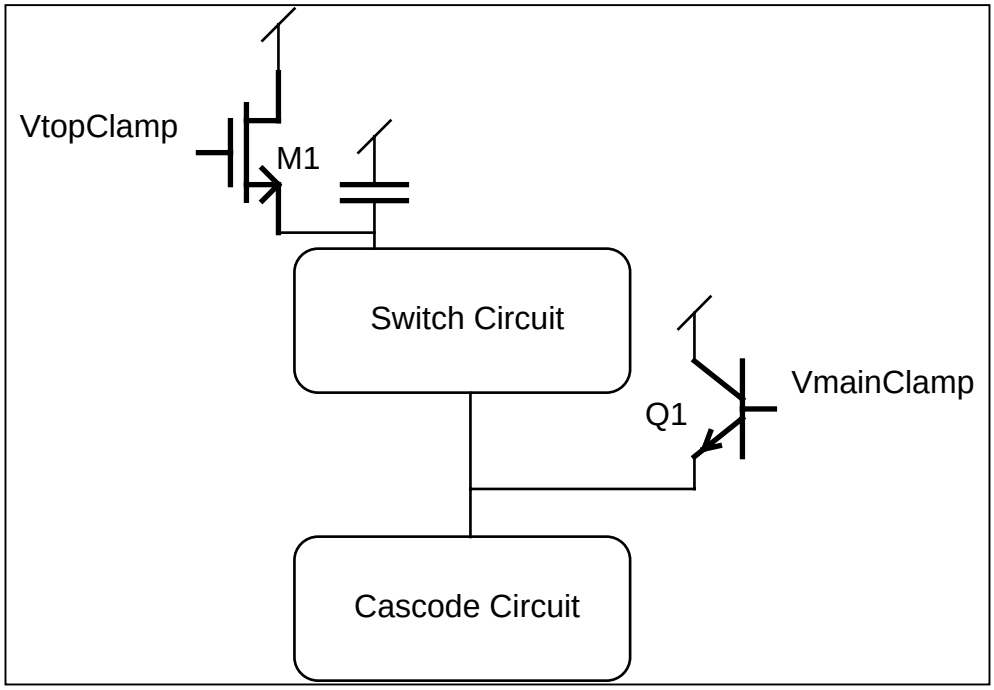

Figure 11: The Dump Circuit

The Dump Circuit, shown in Figure 11, takes the form of two clamps, one at each integrating capacitor (the Top Clamp) and one between the Cascode and Switch Circuits (the Main Clamp). When the voltage across the integrating capacitor reaches approximately one threshold voltage below VtopClamp, then the Top Clamp Transistor (M1 in Figure 11) will begin to conduct current. Up to that point, M1 was off and was not interfering with circuit operation. As more charge is integrated onto the capacitor, M1 will turn on harder and conduct more current until eventually it was conducting all of the current. This effectively clamps the minimum voltage at the base of the capacitor to one threshold voltage below VtopClamp.

If the input charge is large enough, then it is still possible for the voltage drop across the cascode transistor of the Switch circuit to interfere with proper operation of the Cascode

Circuit and the Splitter. Therefore, the Main clamp is still necessary. Like the Top Clamp, the Main Clamp transistor (Q1 in Figure 11) will turn on when the voltage between the Switch and the Cascode reaches one diode drop below VmainClamp.

It is important to realize how the Top Clamp and the Main Clamp work together to ensure proper operation of the circuit. If there were no Main Clamp, it is still possible to destabilize the operation in the Cascode and Splitter. If there were no Top Clamp, then when Main Clamp turned on, all current would flow through the Main Clamp circuit after it turned on, even the bias current. No current would have to flow through the Switch. This would starve the Switch Circuit for current and it would take a very long time for the voltage between the Switch and the Cascode to rise above the clamp voltage.

Under proper operating conditions, the Top Clamp turns on first. Current must flow through the Top Clamp until the voltage at the bottom of the integrating capacitor goes above the clamp voltage. If excessive charge also causes the Main Clamp to turn on to protect the Cascode and Splitter circuits, not all of the current would flow through the Main Clamp. Some current must still flow through the Top Clamp because, by definition, the voltage at the bottom of the integrating capacitor is still at the clamp voltage. Therefore, the Switch circuit cannot be current starved and the Front End will recover as soon as the excessive input charge goes away.

By definition, the two bias voltages, VtopClamp and VmainClamp will be very process dependent, especially the former. Moreover, VmainClamp will draw current since it is the

base of a bipolar transistor. The bias circuitry should take this into account. Both biases should be brought out to pads.

3.6 Integrating Capacitors

The requirements on the integrating capacitor are very straightforward. It needs to be reproducible across all ranges. Therefore, a poly-poly capacitor is best because the thin oxide is better controlled than the thicker field oxide. It must be independently resettable. Therefore, each capacitor needs its own reset transistor. It will be reset to the positive voltage rail. Therefore, the reset transistor should be a pfet and not an nfet. The only question that remains is what size it must be. The answer to this question can be found from the stated resolution requirements.

It is required that the Least Significant Bit resolution on the I/2 Range be 12.5 fC[2]. This means that the entire I/2 Range covers 400 fC since there are five bits in the mantissa. The Splitter Output Voltage Swing is the output voltage of "interesting" charges. It is specified to be between 3 and 4 volts[3]. Since the I/2 range is "interesting" for charges between zero and 400 fC, the calculation of capacitance of the integrating capacitors is very straightforward. Q=CV and C must be 400 fF if Q is 400 fC and V is 1 volt.

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[2] "Specifications for the Shower Max QIE" by G. Drake April 30, 1997 available at "http://www-cdf.fnal.gov/runII_spec/spec_smqie.txt"

[3] Ibid.

Furthermore, it is possible to calculate the allowable splitter bias current in a similar fashion. The integrating capacitor will be reset to the positive rail, which is 5 volts[4]. If there is no input charge, the Splitter Output Voltage must be 4 volts. Therefore, the Splitter Bias Current must integrate one volt across a 400 fF capacitor in 132 ns. I=C(dV/dT), and C is 400 fF, dV is one volt and dT is 132 ns. Therefore, the Splitter Bias Current I must be 3 μA.

Note that the 400 fF of the integrating capacitor take into consideration not only the desired capacitance of the poly-poly capacitor, but also the following:

1. The poly-poly fringe capacitance
2. The reset transistor drain capacitance
3. The Switch circuit switch transistor drain capacitance (M4-M7 in Figure 10)
4. The Top Clamp transistor drain capacitance
5. The Range Comparator gate capacitance
6. The Analog Output gate capacitance
7. Routing parasitic capacitance

3.7 Excess Current

The 3 μA of Splitter Bias Current permitted by the Splitter Output Voltage Swing requirements is not enough to ensure proper functionality of the front end. The Splitter itself, which behaves from this perspective like one large bipolar transistor, will have an input impedance of over eight kΩ. Taking into account the effect of the Splitter Feedback Amplifier, the absolute input impedance of the Front End would be between 200 and 1000

[4] "Specifications for the Shower Max QIE" by G. Drake April 30, 1997 available at http://www-cdf.fnal.gov/runII_spec/spec_smqie.txt.

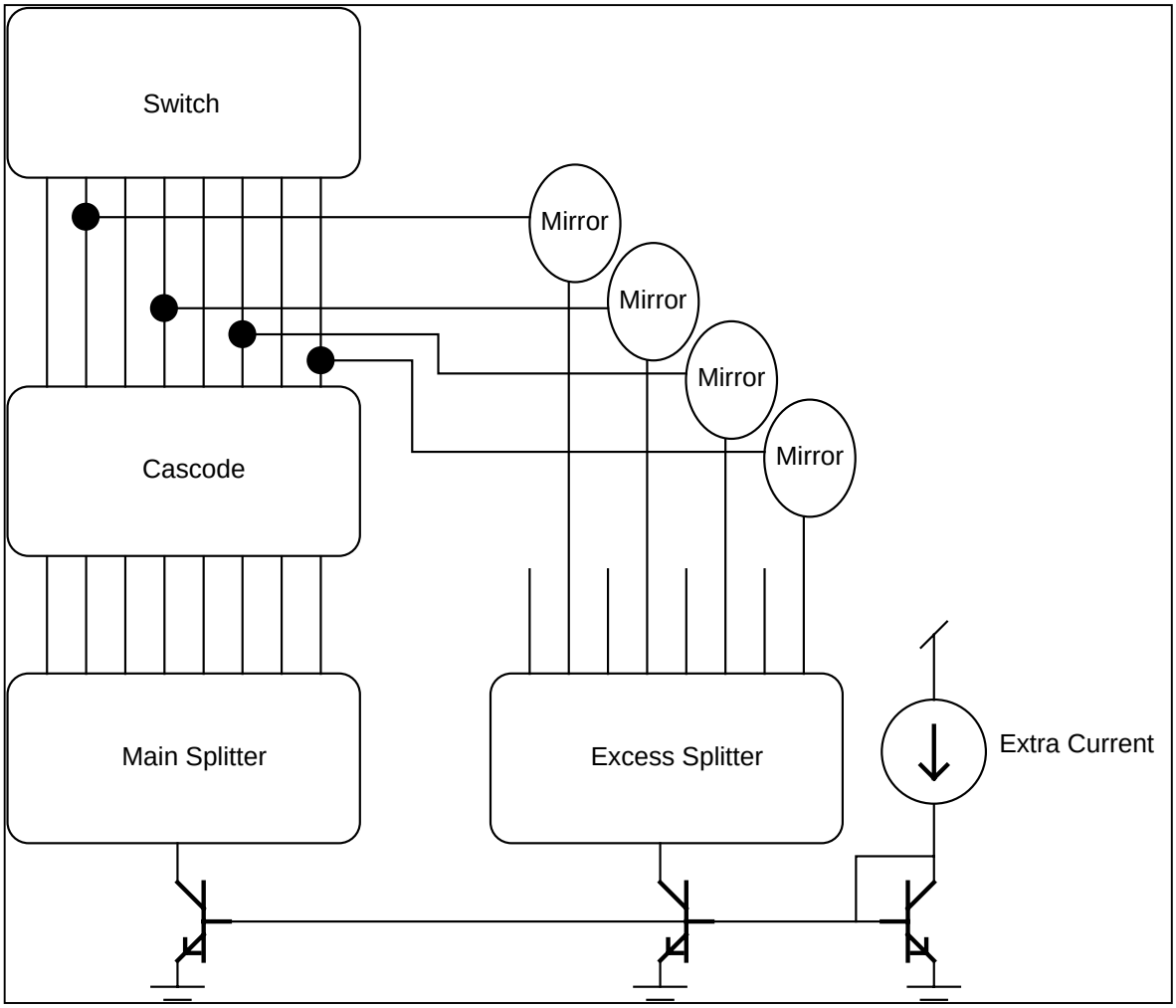

Figure 12: The Excess Current Configuration

ohms. This is too high. Moreover, with only 3 μA flowing through the Cascode circuit's cascode transistor, the performance of the Splitter's collectors would be sluggish as well. Therefore, some way of injecting excess current into the splitter, but extracting it prior to the integrating capacitors is necessary. This injection and extraction is more difficult than it sounds. While it is possible to inject one current at the input of the Front End, eight exact,

binary-scaled currents, whose sum equals the injected current, must be extracted before they reach the integrating capacitors.

This is accomplished in the SMQIE by the addition of a second Splitter circuit and eight high-output impedance, pfet cascode current mirrors. The second splitter only accepts the excess current as its input. It splits the excess current and delivers it to the current mirrors. The pfet mirrors reflect the current and extract it below the Switch Circuit. Perhaps, it would have been preferable to extract the current directly below the integrating capacitors, but then it would have been necessary to have 32 mirrors (eight ranges times four phases). The excess current mirrors would also contribute to the parasitic capacitance on the integrating capacitor. Most importantly, the excess current mirrors would have had to "know" not to extract current except during the integration phase. Therefore, it was decided to place the extraction point below the switch circuit.

The Excess Current Circuitry is shown in Figure 12. For readability, the different circuit elements were represented symbolically, and four of the mirrors were not drawn. In the SMQIE, there is one mirror for each of the eight ranges.

3.8 Range Selector

The preceding sections showed how an injected charge could be split into eight binary-scaled ranges and then each range reliably and reproducibly integrated onto one of four capacitors. For every possible charge between zero and the maximum allowable input charge, there will be a unique voltage signature on the range capacitors. This unique signature must be evaluated by the Range Selector to determine which range is appropriate.

3.8.1 How it works

The Splitter Output Voltage Range of 3 to 4 volts was not arbitrarily chosen. The low voltage end (3 volts) is twice as far from the 5 volt power rail (the capacitor reset point) as the high voltage end (4 volts). Therefore, it takes twice as much input charge, including the Splitter Bias Current, to integrate a particular range to 3 volts as it does to integrate it to 4 volts. This is nothing more than the basic physics of a capacitor, Q=CV. If $Q_1=CV_1$ and $Q_2=CV_2$, and if V_1 is twice V_2, then Q_1 is twice Q_2. This selection of the Splitter Output Voltage Range was designed to mate with the binary-scaled range currents being delivered to the integrating capacitors. Range X has half the current of Range X-1. Therefore, the voltage at the anode of Integrating Capacitor X will just be reaching 4 volts as the voltage at the anode of Integrating Capacitor X-1 will be reaching 3 volts. The voltage at the anode of Range X-2 will be below 3 volts and the voltage at the anode of Range X+1 will be above 4 volts. Simply put, then, the appropriate range for a given input charge is the only range whose integrating capacitor has its anode between 4 and 3 volts. The offset voltage, i.e. the voltage that will be fed into the flash and will become the mantissa, is the only voltage at the anode of a range capacitor that is between 4 and 3 volts. The job of the Range Selector is to pick that capacitor.

3.8.2 The Range Comparator

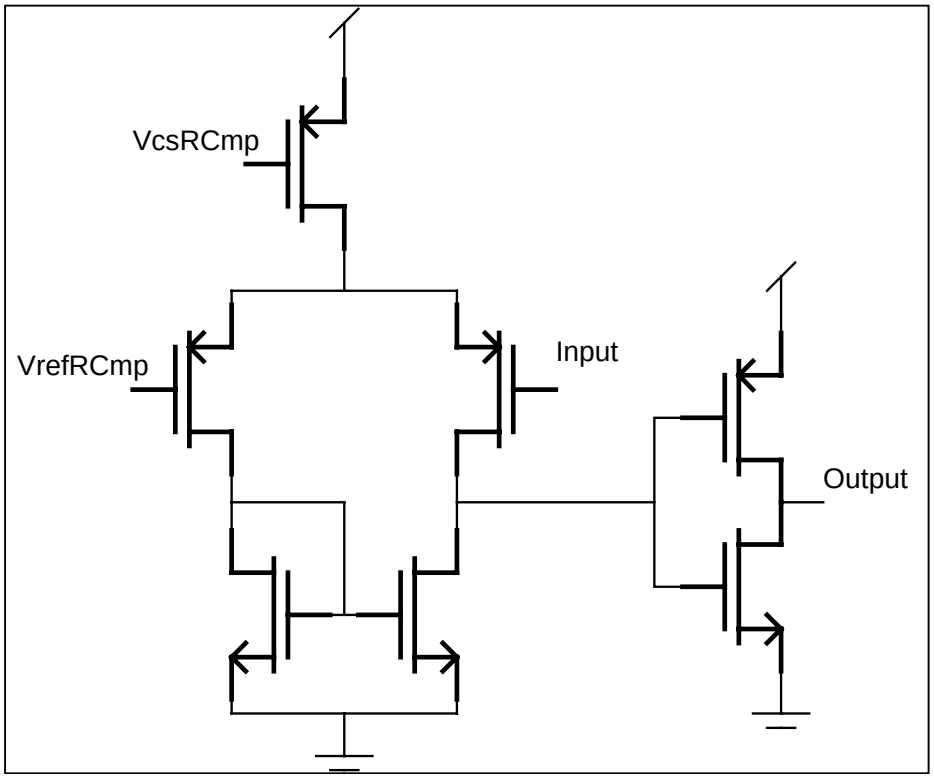

Figure 13: The Range Comparator

The SMQIE Range Comparator is a simple pfet-input differential amplifier with an nfet active load. The output of the differential amplifier drives a simple inverter which provides a rail-to-rail digital signal that is zero if the input voltage has gone below the reference voltage and one if it has not.

3.8.3 Thermometer Code and Selection

From the previous section, if the Range Comparators trip point, VrefRCmp, is set to 3 volts, then the outputs of the eight Range Comparators will be a series of Ones followed by a series of Zeroes. The Ones, obviously, will be for those ranges that have not yet gone

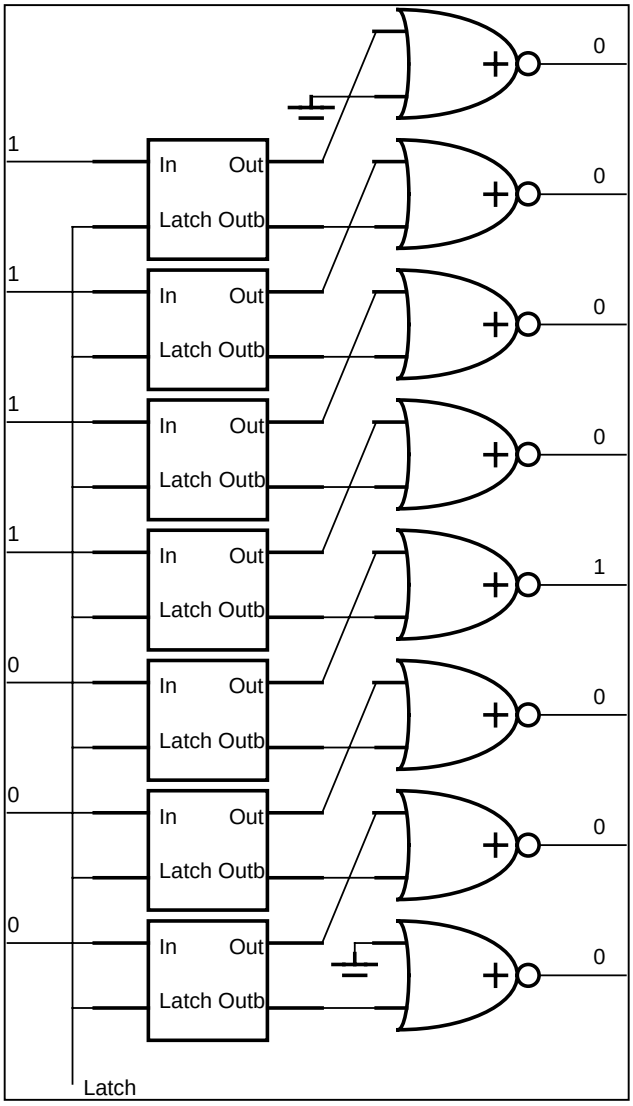

Figure 14: The Range Selection Logic

below three volts. The last One before the series of Zeros will be the capacitor whose anode is between 4 and 3 volts. This type of binary code is called a Thermometer Code because of the way it resembles the mercury rising in a thermometer. In the case of the SMQIE, it has only 8 possible values, 00000000, 10000000, 11000000, 11100000, 11110000, 11111000, 11111100, 11111110, and 11111111. These values represent,

respectively Range 7 (I/256), Range 6 (I/128), Range 5 (I/64), Range 4 (I/32), Range 3 (I/16), Range 2 (I/8), Range 1 (I/4) and Range 0 (I/2).

This thermometer code must be latched at an appropriate time and then converted into a more useful binary code, the Signature Code, that only has one active signal. Like the Thermometer Code, it has only eight possible values, 10000000, 01000000, 00100000, 00010000, 00001000, 00000100, 00000010, and 00000001. Each bit of the Signature Code is generated by NORing the logical inverse of that thermometer code bit with the thermometer code bit of the next lower range. This is shown in Figure 14. The lowest range grounds the "next lower range" input of the NOR gate so that if all of the Range Comparators are above 3 volts, then Range 0 is selected by default. The highest range grounds the "logical inverse of the thermometer code" input so that if an extremely high charge is recorded such that all Range Comparators are below 3 volts, then Range 7 is selected by default. The new Signature Code (shown on the right in Figure 14) is then passed to an encoder, which converts it to a 3-bit binary value.

Note, there must be one set of eight range comparators and one set of the range comparator logic as shown in Figure 14 for each of the four phases provided by the Switch Circuit.

3.9 Analog Output

After the Range Selector has picked a particular range, the analog output must be released to the Flash Converter. This is accomplished in a unique way in the SMQIE. Using the same Signature Code that is passed to the Range Encoder, the appropriate piece of a distributed unity gain amplifier is activated.

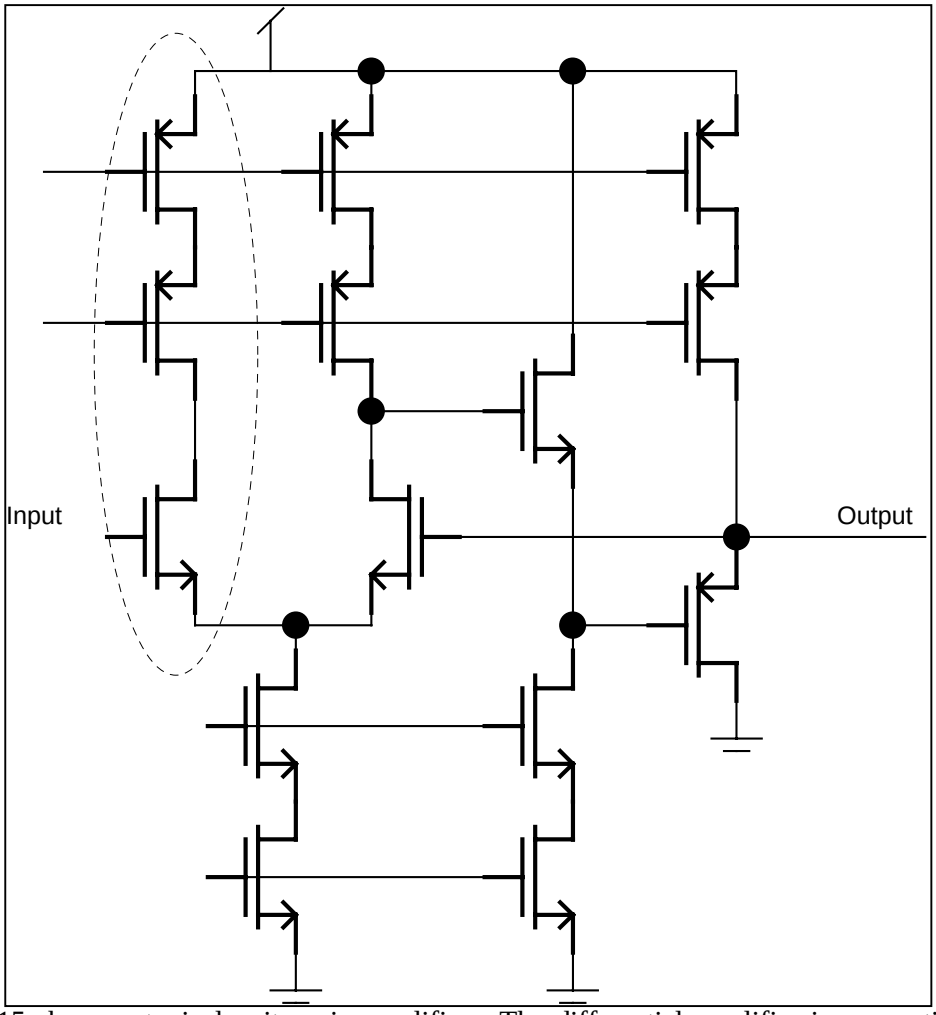

Figure 15 shows a typical unity-gain amplifier. The differential amplifier in a negative feedback configuration tries to keep the output equal to the input. The four bias voltages, which set the currents, can all be established from a single resistor by using one nfet and

Figure 15: A typical unity-gain amplifier

one pfet current mirror. The modification used by the SMQIE is to eliminate the three transistors in the dotted oval and replace them with eight selectable branches. This is shown

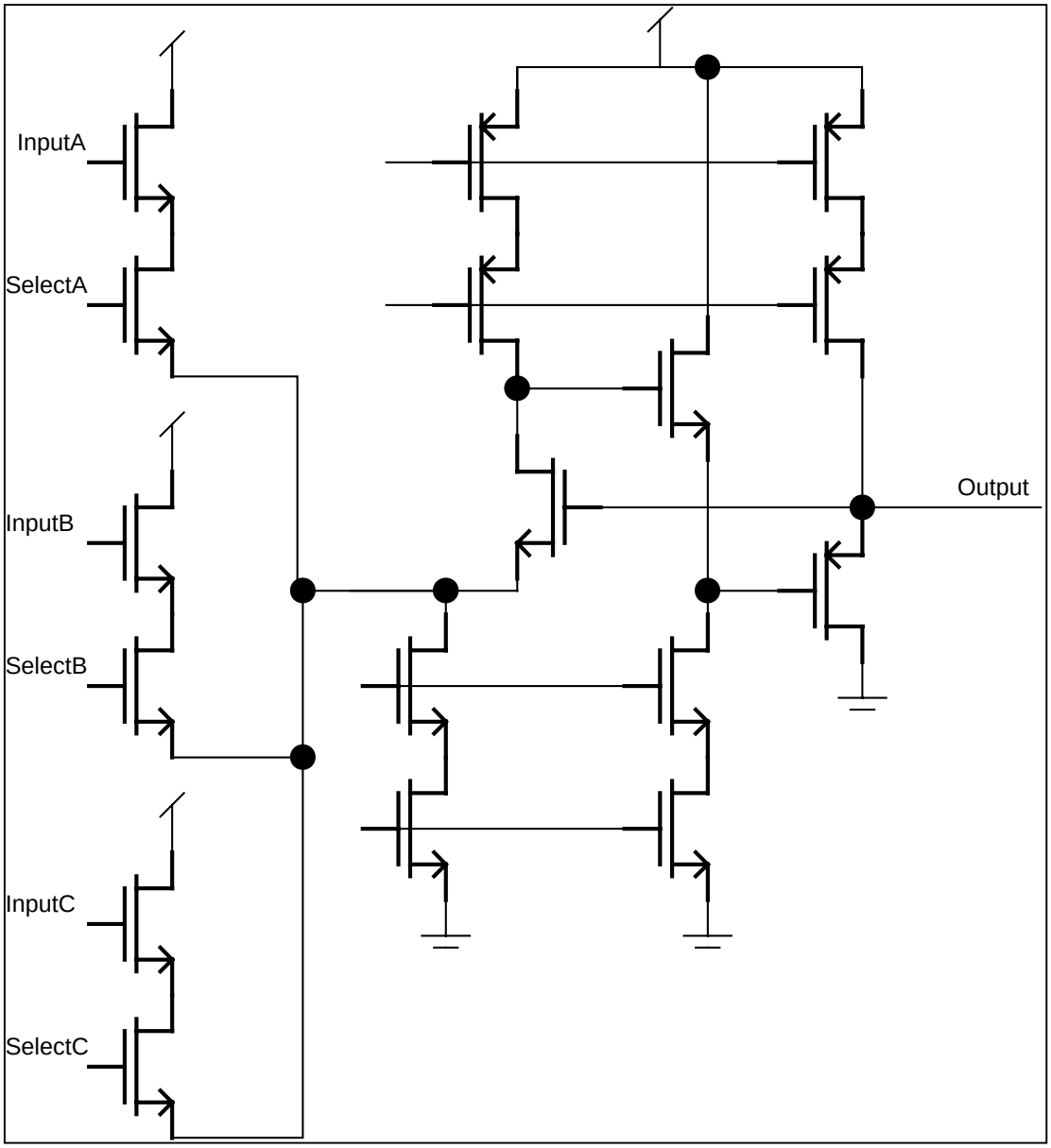

Figure 16: A distributed unity-gain amplifier with three inputs

in Figure 16. These selectable branches are located by the integrating capacitors in the layout. The remainder of the analog output circuit is located elsewhere.

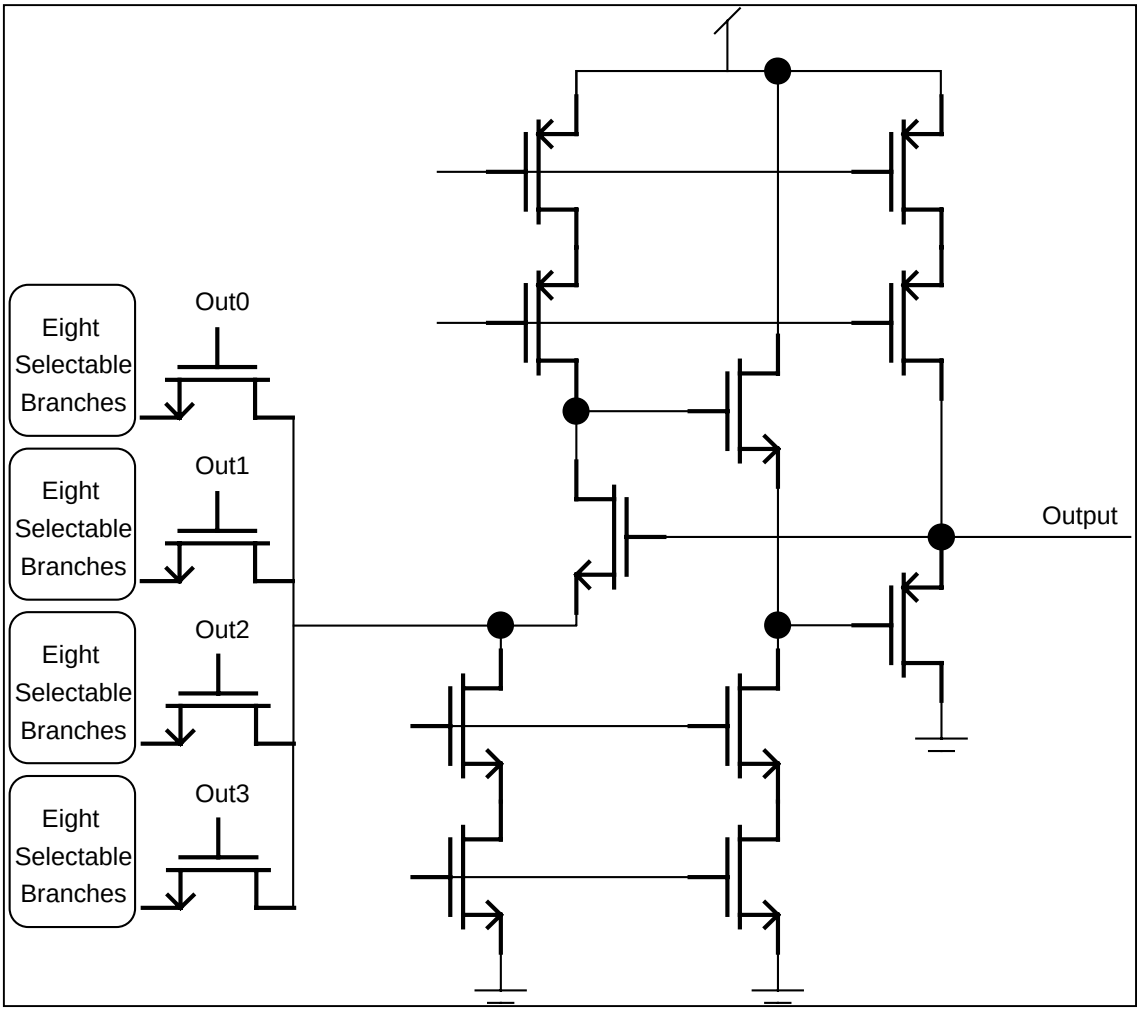

Figure 17: A distributed unity-gain amplifier with 32 inputs in four phases

In fact, the SMQIE is forced to take this distributed unity-gain amplifier a step further. Recall that there are four sets of eight Range Comparators and four sets of Range Selection logic corresponding to the four Integrating Capacitors per range. The analog output circuitry must have the ability to select one of the four phases as well as the ability to chose which range to output. This is shown in Figure 17.

3.10 Four Phase Clock

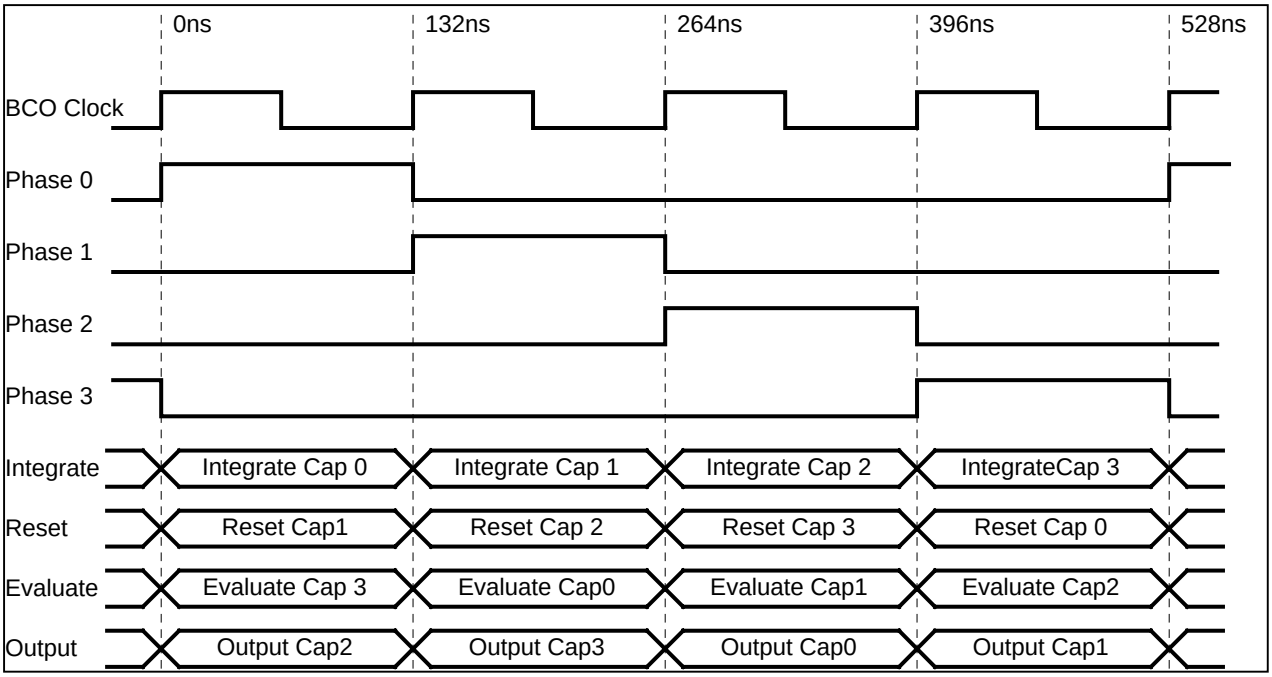

Figure 18: Basic Four Phase Process

In the preceding sections, mention was made of four phases and signals which controlled certain operations. These signals are provided by the Four Phase Clock. Again, the four phases are necessary because an incoming signal must be integrated onto a capacitor; it must be evaluated; and the result must be output. Finally, the capacitor must be reset. Since the chip must operate with no dead time, there must be four capacitors so that each function (Integrate, Reset, Evaluate and Output) can be operating on one and only one of the capacitors at any given time. This is shown in detail at the bottom of Figure 18.

The top of Figure 18 also shows how the SMQIE achieves this objective. The BCO Clock advances a simple four-element ring counter formed from one settable and three resettable,

positive edge triggered D-flip flops. The outputs of these four flip-flops give a reliable, reproducible indication of which phase the current phase of the Front End. Simple combinatorial logic converts the phase signals into the necessary functional signals.

The necessary function signals are actually four sets of four signals. Two of these sets, Integrate and Output, must operate over the entire 132ns time slice. The other two cannot. Reset cannot be permitted to operate near the clock edges because of the chance that spurious delays in the combinatorial logic or in the routing might cause accidental resets of the wrong phase. Resetting can only be allowed in the middle of a phase. Moreover, since Reset must activate the gates of pfet transistors, it must be negative active. Evaluate, as a function, is not truly necessary. It is obvious from the section on the Range Selector that the Range Comparator is operating at all times. What is necessary is that the thermometer code of a particular phase be latched into the flip-flops after a sufficient time has passed to allow the comparators to do their job. Therefore, a Latch signal set is necessary that will be active only at the end of each Evaluate phase.

In order to accommodate the two signal sets that require only portions of a time slice, a delayed clock is formed by passing the real clock through a series of 20 inverters. This delayed clock is NANDed with the real clock and NORed with the real clock. The Nor Clock is active only at the end of the time slice and the Nand Clock is active only for a short period of time in the middle of the time slice. The Nand Clock and the Nor Clock are combined with the phase signals to create the 16 required functional signals. This is shown in Figure 19.

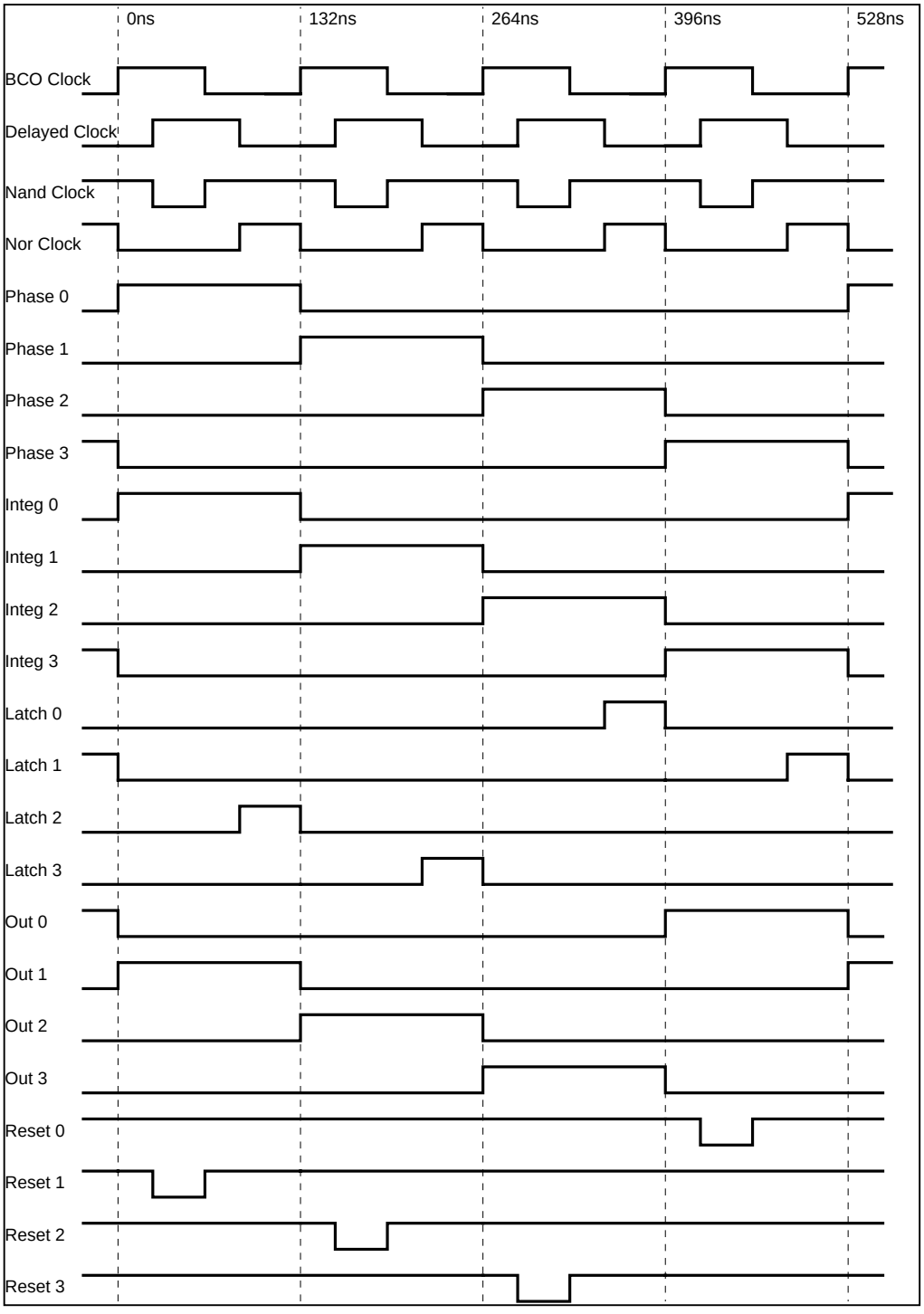

Figure 19: Basic Four Phase Process

4 The Flash

Logically, the Flash is similar to the Range Selector Logic. Recall that in the Range Selector, eight unique voltages from the eight integrating capacitors are compared against one comparator trip point, VrefRCmp. This generates an eight-bit thermometer code, which is converted into an eight-bit signature code with only one active bit. The signature code is used to release the appropriate analog output and is encoded into a binary value. In the Flash, a single input voltage (the analog output of the Front End) is compared to 31 unique reference voltages. This generates a 32-bit thermometer code, which is converted into a 32-bit signature code with only one active bit. The signature code is finally encoded into a 5-bit mantissa.

4.1 The Reference Voltages

The Flash needs a way to provide 31 reliable and reproducible reference voltages without getting them externally. The best way to do this in VLSI is to use a resistive divider because, while the absolute value of a particular resistor in an integrated circuit can vary by ±25%, the relative value of two or more resistors should track to better than 3%. Of course, this really only works if the voltage references are not required to provide a lot of current, so this presents a limitation on the types of comparators that can be used.

Since the analog output of the Front End is between 3 and 4 volts, the Flash references need to be evenly spaced from 3 to 4 volts. Five identical resistors in series between power and ground will provide four stable voltage references at 1-volt, 2-volts, 3-volts, and 4-volts. If the resistor between 3 and 4 volts is subdivided into 30 identical resistors, the result is 31

stable, low-current voltage references between 3 and 4 volts. This can be easily accomplished in VLSI using either polysilicon or diffusion as the resistor material. Polysilicon was chosen for the SMQIE. Five resistors, each approximately 2.64 kΩ were placed between power and ground. One of these resistors was further divided into 30 identical resistors of 88 ohms each (30 x 88 = 2.64 kΩ). This translates to an additional 2.4 mW quiescent power requirement on the circuit to account for the current that will flow between power and ground.

For additional stability, VladTop (4 volts) and VladBot (3 volts) are brought out to pads so that they can be connected to bypass capacitors. This also provides a very low level, sanity check on the fabrication. If VladTop and VladBot are 3 volts and 4 volts, respectively, then, at the very least, the chip has polysilicon, metal 1 and contacts. This may seem ridiculous to those unfamiliar with our semiconductor manufacturer, but suffice to say that the SMQIE team has needed this check in the past. The VladTop and VladBot pads also provide a way to override the Flash rails if necessary.

4.2 The Flash Comparator

The Flash Comparator uses a simple pair of cascaded CMOS inverters. While less precise than high-end comparators, this style uses considerably less power and space. Since the flash will use 32 comparators, both power and space are very important. Furthermore, the Flash Comparator divides the BCO clock cycle into two phases – set-up and convert. To do this it requires three related clock signals, SwtIn, SwtRef, and Reset, all of which are derived from the clock input. The architecture is shown in Figure 20.

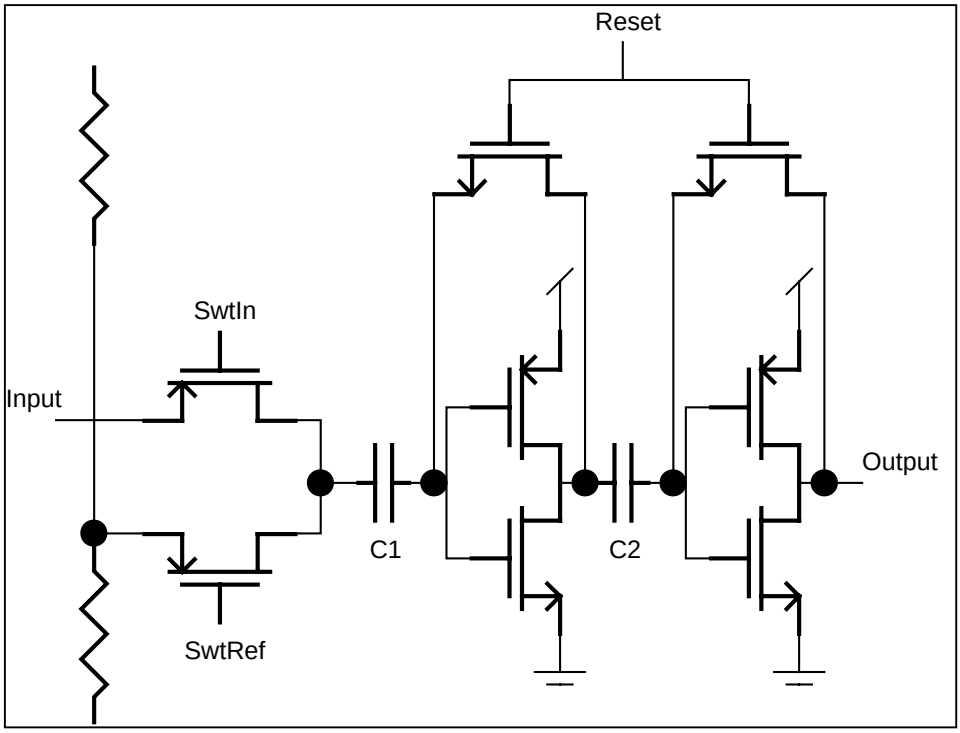

Figure 20: The Flash Comparator

When Reset is held active, the input and output of each inverter are equal. This means that both transistors in each inverter are in saturation (Vgs = Vds) and the inverters are at their trip points. This is the point of maximum gain for a CMOS inverter. Any difference between their two trip points would be stored as a charge on the capacitor, C2. Such differences could arise from layout variations or process variations such as threshold voltage shift. The presence of the C2 Capacitor helps minimize offset variations that will arise in such a simple comparator.

During the set-up phase (the first half of the clock cycle), both Reset and SwtRef are held active. Therefore, C1 will store a voltage equal to the difference between the trip voltage of the inverter and the reference voltage (Vtrp – Vref). During the evaluate phase, both Reset

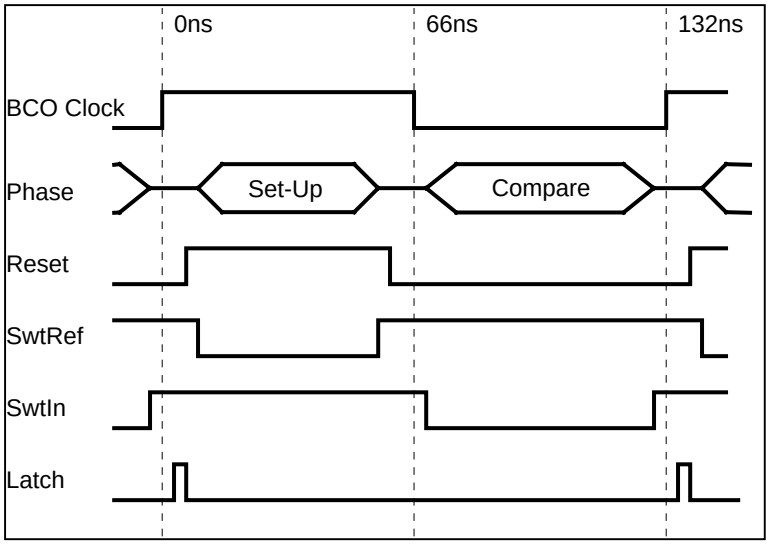

Figure 21: Flash Clock Logic

and SwtRef are made inactive and SwtIn is made active. When this occurs, the voltage at the input of the first inverter is equal to the input voltage plus the voltage stored on the capacitor, C1. That is to say, the input voltage of the first inverter is equal to the trip voltage plus the difference between the input voltage and the reference voltage. The gain of the two inverters in series is approximately 100. Therefore, the difference between the input and reference voltage is amplified, and the comparator is forced to output either a One (if Vin > Vref) or a Zero (if Vin < Vref).

Finally, at the next rising edge of the clock, the outputs of the comparators are latched and passed through an encoder similar to that used in the Range Selector. The timing is shown in Figure 21.

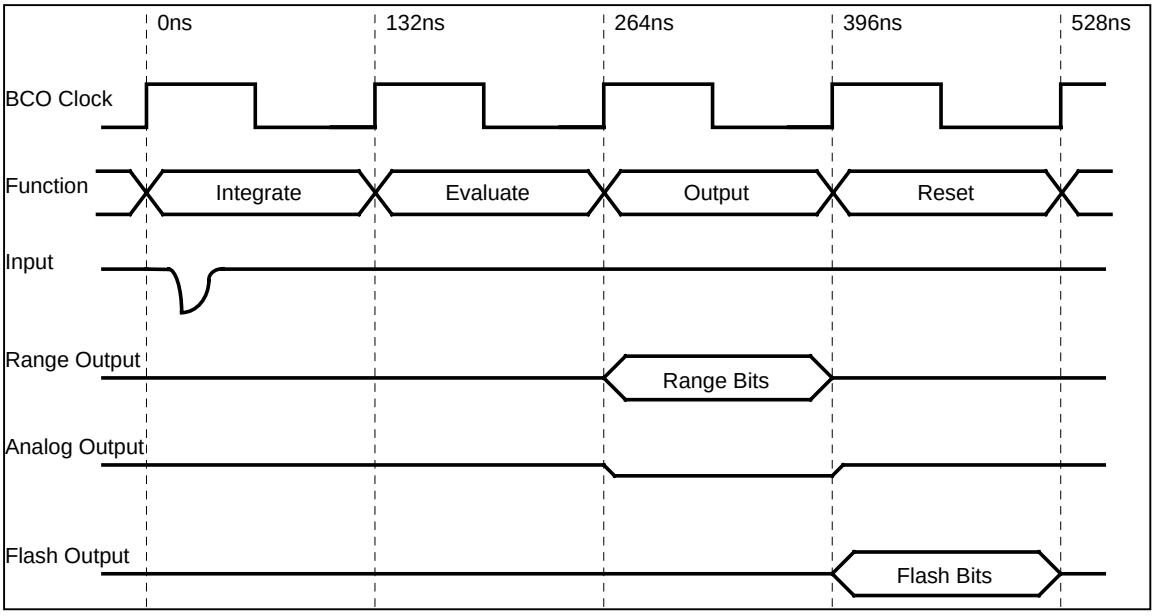

Figure 22: Basic Four-Phase Process

5 The Back End

5.1 Synchronizer

Figure 22 shows a picture of the evolution of an event. An input occurs during the Integrate phase of one of the capacitors. During the capacitor's second phase, the input is evaluated by the Range Selector. During the Output phase, the three Range Bits and the Front End's Analog Output are output. Finally, during the forth phase, while the capacitor is being reset, the Flash Outputs the five mantissa bits. This all works rather well, except for the fact that the output of an event, which occurred in a single time slice, is spread out over two time slices. To make matters worse, a cyclical Capacitor Identification or CapID is derived from the four Integrate signals. This information must be passed along with the Range and Flash bits to help downstream data processing elements verify that the SMQIE

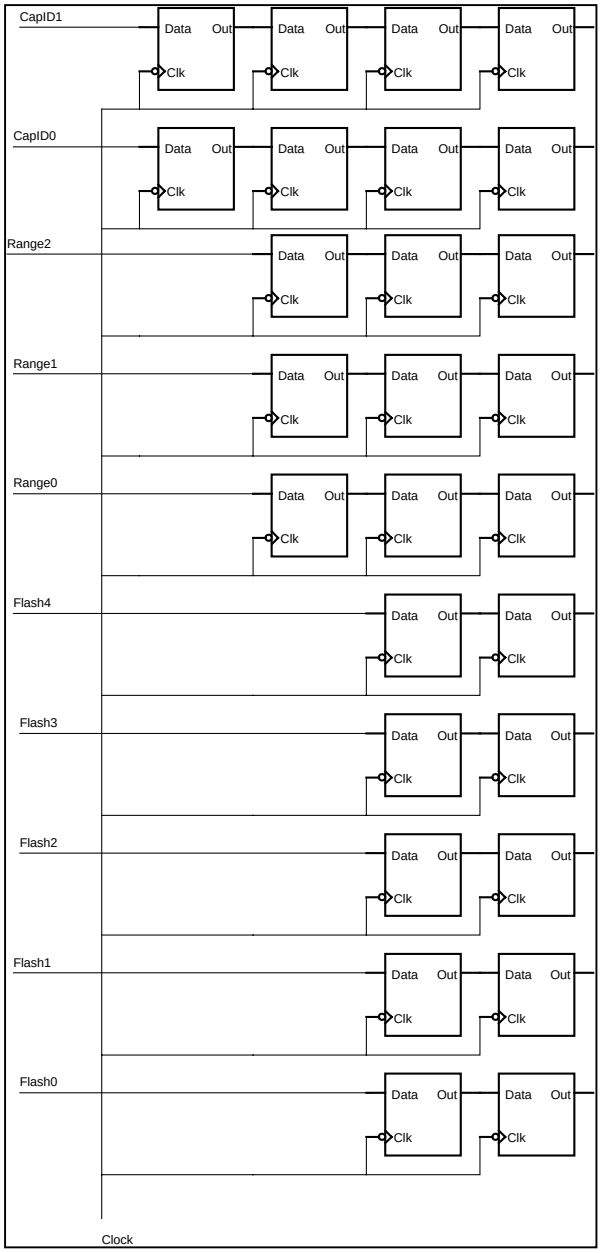

Figure 23: The Synchronizer

is function properly and that data is being transmitted without errors. Therefore, in reality, an event, which occurs in one time slice, generates output over four time slices. The

information needs to be aligned into one digital word and this is the function of the synchronizer.

Note that in Figure 22, information, regardless of whether it is CapID, Range or Flash bits, changes state on the rising edge of the clock. It is stable on the falling edge of the clock. Therefore, at the falling edge of every clock, two CapID bits, three Range bits and five mantissa bits are latched into ten edge-triggered D-flip flops. See Figure 23. The mantissa bits must pass through a two-stage deep FIFO; the range bits must pass through a three stage-deep FIFO; and the CapID bits pass through a four stage-deep FIFO. All of the FIFOs are synchronized to the BCO clock and they change state at the falling edge. The output of the synchronizer is a 10-bit wide word that contains all the CapID, Range and Flash bits of a single event. [Note: In truth, the CapID synchronization is incorrect. The phase X Flash and Range bits are synchronized with the phase X+1 CapID bits. However, it was decided not to change this error. Downstream CapID checking only verifies that the capacitors are cycling from 0 to 1 to 2 to 3 and back to 0. Since this type of check is still valid despite the presence of the error, the risk associated with altering the chip was more important than fixing a cosmetic error.]

5.2 Level 1 FIFO

Though it represents a very significant percentage of the area of the chip (almost 10000 transistors), the Level 1 FIFO is actually very simple. It is a 10-bit wide, 38-stage deep FIFO. All elements of the FIFO are synchronized to the falling edge of the BCO clock. The outputs of the 38^{th}, 37^{th}, 36^{th}, and 35^{th} stages are made available to the Level 2 buffer area.

5.3 Level 2 Buffer

The Level 2 Buffer holds up to four sets of four time slices of data. The data includes the two CapID bits, the three Range bits, the five Mantissa (Flash) bits, and a Parity bit. Four time slices of data are required per set so that SMQIE will work for both the Central and the Plug Calorimeters. Recall from the Introduction that the Central Shower Max detector uses slower strip chambers that will output charge for four time slices per event. The SMQIE could be required to sum the charge from four events, but data from fast photomultiplier tubes in the Plug detector must not be summed. To reduce the cost of fabrication and have one SMQIE for both applications, the solution is to have the downstream data acquisition systems view the SMQIE as a memory. The downstream data acquisition system must know if a particular SMQIE is gathering data from a Plug or Central detector. If it is a Plug SMQIE, then only the first time slice is necessary. If it is a Central SMQIE, then four time slices per buffer number must be requested.

In addition to the four time slices from the Level 1 FIFO, the Level 2 Buffer will need some additional information from the outside. To write a Level 2 Buffer, it requires a Level 1 Trigger to indicate when a particular time slice is interesting. It must also know into which of the four buffers it must put the information. When it receives a Level 1 Trigger and a Write Buffer Number, at the falling edge of the BCO clock, the Level 2 Buffer latches the output of 38^{th}, 37^{th}, 36^{th}, and 35^{th} FIFO stages of the Level 1 FIFO into the TS0, TS1, TS2 and TS3 (respectively) registers of whichever buffer is chosen. To read a Level 2 Buffer, the buffer number and the time slice are all that is required. Reading is asynchronous.

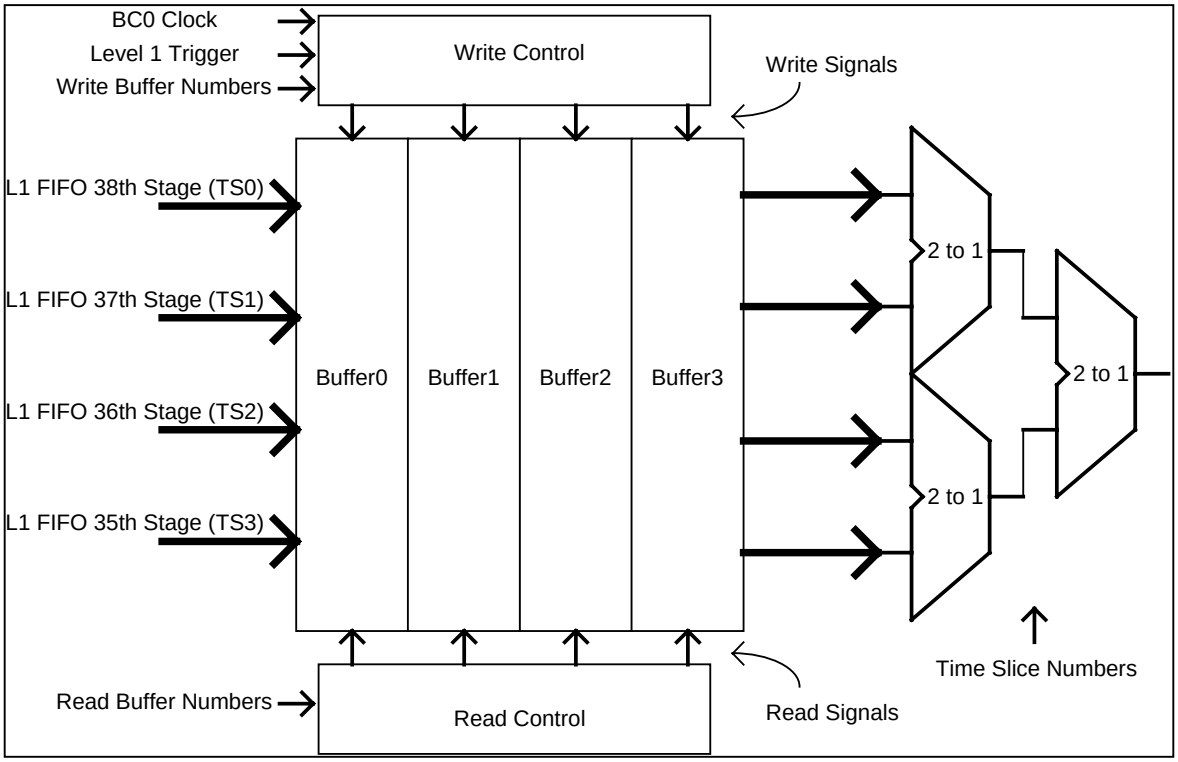

Figure 24: Level 2 Buffer Architecture

Note that the Level 2 Buffer is stupid. It will happily overwrite the same Level 2 Buffer every time it receives a Level 1 Trigger if the Write Buffer Number is not changed. It does nothing to prevent data corruption or data loss. It will also joyfully write to the buffer the user is trying to read if the user has both the Read and Write Buffer Numbers set to the same number.

5.3.1 Parity

The data acquisition system uses the Parity bit as a simple means to verify that it has received uncorrupted data. It is formed from the three Range bits and the five Mantissa

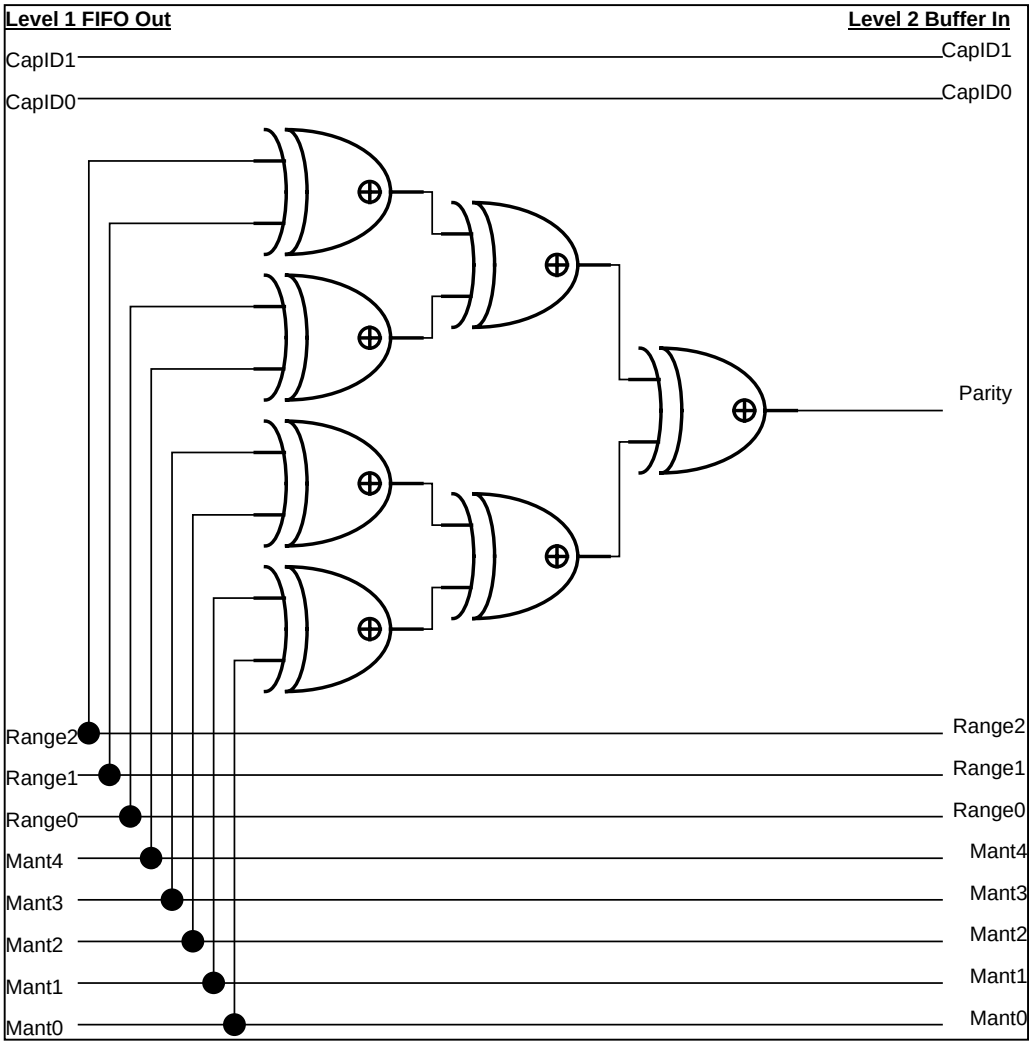

Figure 25: Parity Generation

bits. To simplify the design, it was decided not to include the CapID bits in the parity check since a corrupted CapID bit will be flagged by the data acquisition system anyway.

The SMQIE uses a simple exclusive-or-based even parity. Parity is generated for each time slice of data as it is driven into the Level 2 Buffer, and it is only stored if a Level 1 Trigger is received. Figure 25 shows how parity is generated as well as the final format of the data word.

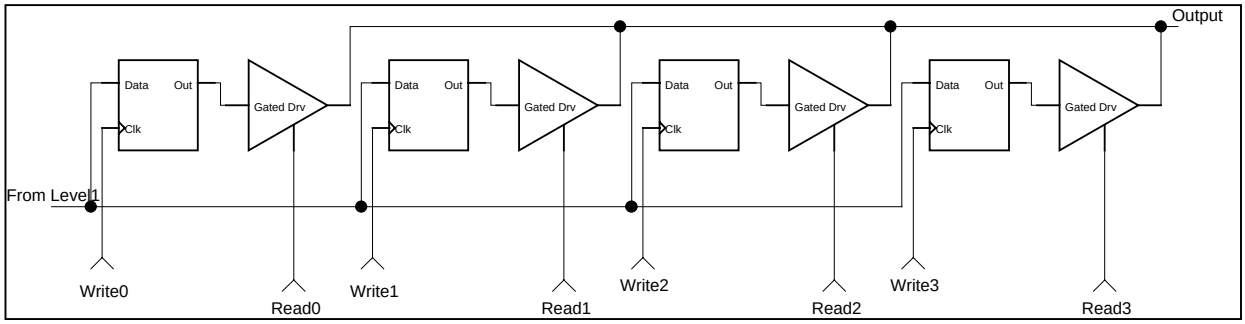

Figure 26: Data Storage Architecture

5.3.2 Data Storage and the Gated Driver

Figure 26 shows in more detail how the Level 2 Buffer appears to each bit of incoming data from the Level 1 FIFO and to the Parity Bit. The falling edge of a Write Signal (Write0, Write1, Write2 or Write3) latches the incoming data into one of the four buffers. The activation – not the edge – of any of the Read Signals (Read0, Read1, Read2 or Read3) will output the corresponding buffer's information. The Gated Driver is shown in Figure 27. It is necessary because only one of the four buffers can be allowed to output its contents at

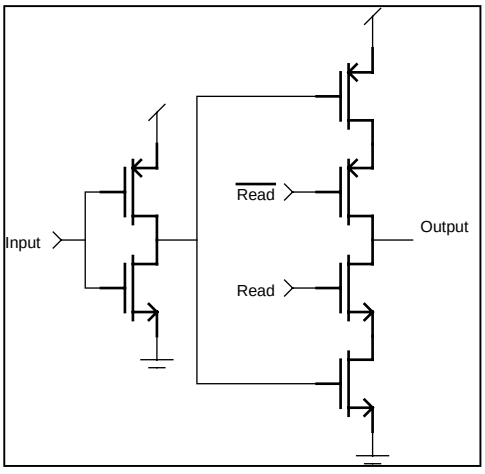

Figure 27: The Gated Driver

any time. Either the buffer's driver must be tri-stateable or a more complicated 4-to-1 multiplexer structure would be required. The Gated Driver solution is just as reliable as the multiplexer while being more compact.

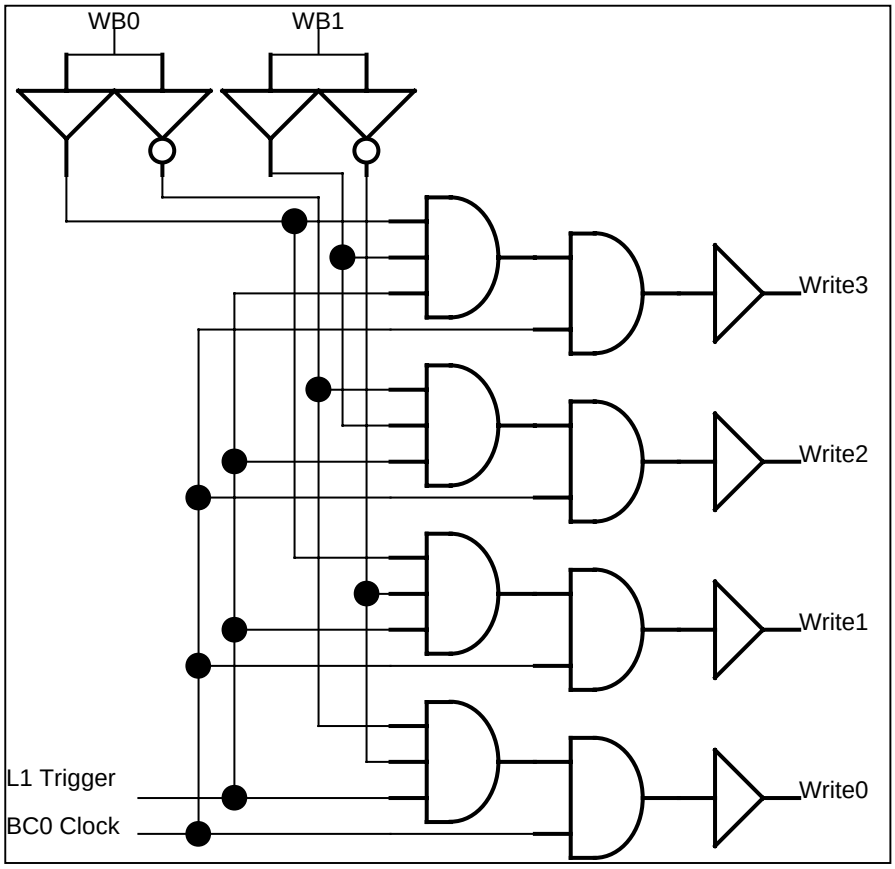

Figure 28: The Write Control Logic

5.3.3 Write and Read Control

The Write and Read Control logic in the SMQIE are virtually identical. The Write Control Logic is shown in Figure 28. The Write Buffer Numbers (WB0 and WB1) are decoded and combined with the Level 1 Trigger signal to create four signals, only one of which is active when the Level 1 Trigger is active. These four signals are combined with the BCO Clock

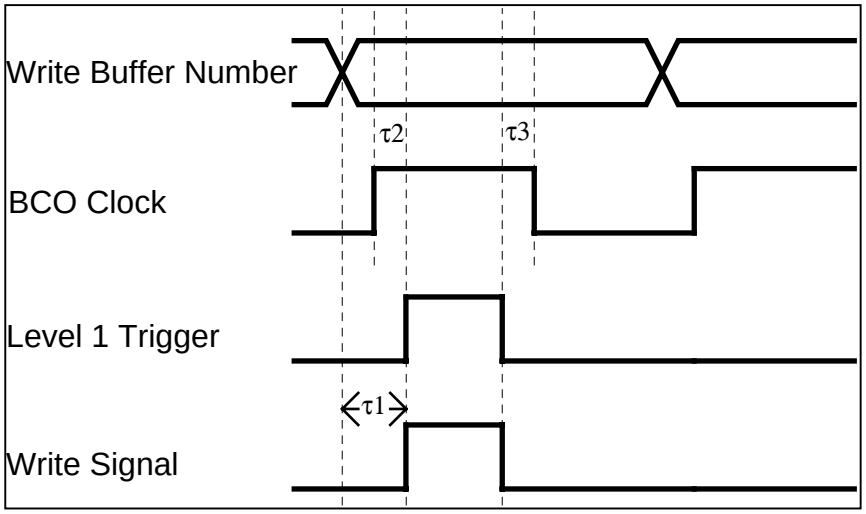

Figure 29: Write Control Timing Considerations

so that the Write Signals will be synchronous with the clock. Recall that the falling edge of the Write Signals will be used to latch the outputs of the Level 1 FIFO into a Level 2 Buffer registers. The falling edge of the BCO Clock is also when data changes in the Level 1 FIFO. Qualitatively, this suggests the timing shown in Figure 29. $\tau 1$, the set up time between the change in Write Buffer Number and the rising edge of the Write Signal, should be greater than the propagation delay through the decoding logic in Figure 28. This is about 1-2 ns. $\tau 2$, the time difference between the rising edge of the clock and the rising edge of the Level 1 Trigger signal is not critical since data is latched on the falling edge of the Write Signals. $\tau 2$ can be as little as zero or as large as 20-30 ns. $\tau 3$ is the most critical time. It should be longer than the hold time of an edge triggered D-flip-flop, approximately 1 ns. However, the BCO clock that is connected to the Level 2 Buffer is delayed from the BCO clock that reaches the Level 1 FIFO by the propagation delay of a large driver (typically 1.5-2ns). Therefore, the $\tau 3$ minimum is met internal to the chip. Simulations of

the chip as well as experiments on the test bench have shown that using the BCO clock as the Level 1 Trigger works without error. In short, due to the logic employed in the SMQIE chip and the manner in which it was laid out, the timing requirements of the Write Control Logic are NOT critical. Board designers do not need to concern themselves with these timing details. However, in the interest of naming a standard, let it be that the Write Buffer Number must reach the chip 2 ns prior to the rising edge of the BCO Clock ($\tau 1 = 2$ ns). The rising edge of the Level 1 Trigger can be coincident with the BCO clock ($\tau 2 = 0$ ns). The falling edge of the Level 1 Trigger must be more than 2 ns before the falling edge of the BCO clock ($\tau 3 = 2$ ns).

The Read Control Logic uses the same circuit shown in Figure 28 except that the Level 1 Trigger and BCO Clock inputs are tied to the power rail. In addition, real and inverted versions of each Read Signal are driven to the buffers.

6 Ex miscelanea

6.1 LVDS Drivers

The SMQIE uses a variation of LVDS-like drivers developed at Fermilab. They are LVDS-like in that they meet the LVDS standard for output voltage levels. However, no attempt was made to meet the standard for output impedance, operating speed, etc. Moreover, the LVDS standard assumes a point-to-point communication protocol. The SMQIE LVDS Drivers can be tri-stated, and therefore can be used when more than one chip is connected to the same bus.

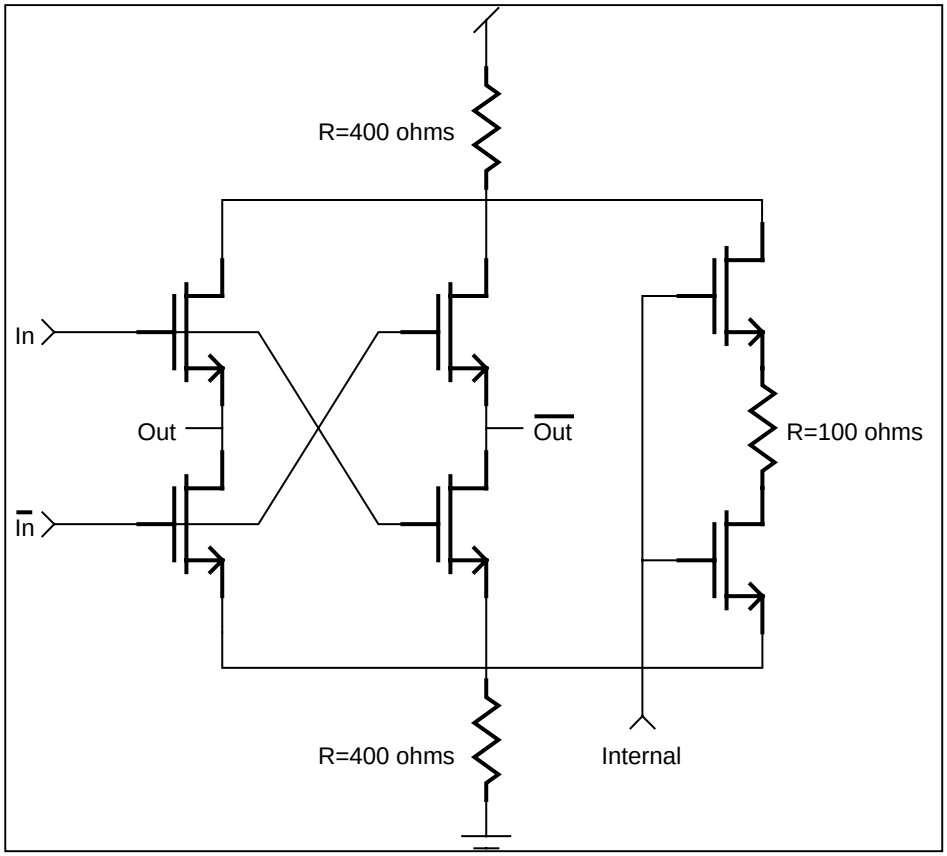

Figure 30: The LVDS Driver

The architecture of the LVDS driver is shown in Figure 30. Under normal operating conditions, Internal is set to zero and the two signal inputs are logical inverts of one another. An externally connected 100 ohm resistance connected between Out and $\overline{\text{Out}}$ conducts current from Out to $\overline{\text{Out}}$ or from Out to $\overline{\text{Out}}$ depending on the logical state of In. When Internal is active, In and $\overline{\text{In}}$ are both set to zero and current is conducted through the internal 100-ohm resistance shown in the figure. The outputs are tri-stated. The LVDS driver uses a special 2.4 volt power supply to make sure that the output voltage swing is around 1.2 volts.

The purpose of the internal signal is to minimize the noise associated with tri-stating the outputs. When the chip is active, as much as 22 mA of current will be flowing from the pad power supply to the pad ground. Interrupting this current flow by tri-stating the chip would cause a ringing in the power supplies that would be seen by the front end.

6.2 Channel Select

In the final version of this chip, there are two channels. A channel consists of one Front End, one Flash, one Level 1 FIFO and one Level 2 Buffer. However, the chip has only one set of data output pads, so a signal must be provided to select between them. This is the Channel Select.

7 Pad Configuration

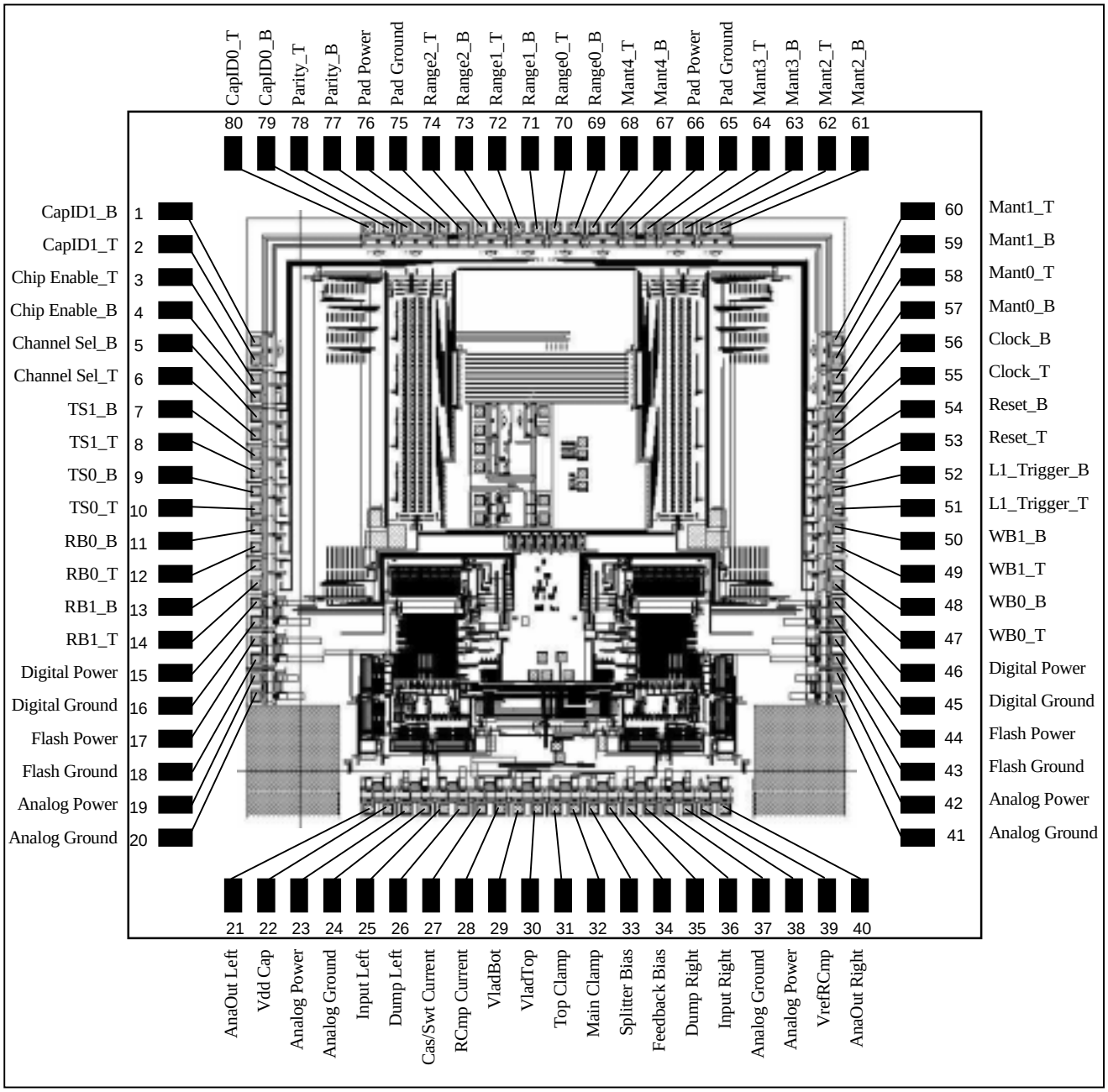

Figure 31: Pad Configuration

Pad#	Pad Name	Pad Type	Descrption
1	CapID1_B	LVDS Out	Most Significant CapID Bit. Connect through 100-ohm load to CapID1_T. V(CapID1_T)>V(CapID1_B) is a Logical 1
2	CapID1_T	LVDS Out	Most Significant CapID Bit. Connect through 100-ohm load to CapID1_B. V(CapID1_T)>V(CapID1_B) is a Logical 1
3	Chip Enable_T	LVDS In	Enables the LVDS outputs. LVDS Levels. V(Chip Enable_T) > V(Chip Enable_B) enables output.
4	Chip Enable_B	LVDS In	Enables the LVDS outputs. LVDS Levels. V(Chip Enable_T) > V(Chip Enable_B) enables output.
5	Channel Sel_B	LVDS In	Channel Select Input. LVDS Levels V(Channel Sel_T) > V(Channel Sel_B) selects the right channel.
6	Channel Sel_T	LVDS In	Channel Select Input. LVDS Levels V(Channel Sel_T) > V(Channel Sel_B) selects the right channel.
7	TS1_B	LVDS In	Most Significant Time Slice Number. LVDS Levels. V(TS1_T) > V(TS1_B) is a Logical 1.
8	TS1_T	LVDS In	Most Significant Time Slice Number. LVDS Levels. V(TS1_T) > V(TS1_B) is a Logical 1.
9	TS0_B	LVDS In	Least Significant Time Slice Number. LVDS Levels. V(TS0_T) > V(TS0_B) is a Logical 1.
10	TS0_T	LVDS In	Least Significant Time Slice Number. LVDS Levels. V(TS0_T) > V(TS0_B) is a Logical 1.

11	RB0_B	LVDS In	Least Significant Read Buffer Number. LVDS Levels. V(RB0_T) > V(RB0_B) is a Logical 1.
12	RB0_T	LVDS In	Least Significant Read Buffer Number. LVDS Levels. V(RB0_T) > V(RB0_B) is a Logical 1.
13	RB1_B	LVDS In	Most Significant Read Buffer Number. LVDS Levels. V(RB1_T) > V(RB1_B) is a Logical 1.
14	RB1_T	LVDS In	Most Significant Read Buffer Number. LVDS Levels. V(RB1_T) > V(RB1_B) is a Logical 1.
15	Digital Power	Power Supply	5.0 volts. Power rail for Level1 FIFO and Level2 Buffer.
16	Dig. Ground	Power Supply	0.0 volts. Ground rail for the Level 1 FIFO and the Level 2 Buffer
17	Flash Power	Power Supply	5.0 volts. Power rail for the 5 bit flash converter.
18	Flash Ground	Power Supply	0.0 volts. Ground rail for the 5 bit flash converter.
19	Ana. Power	Power Supply	5.0 volts. Power rail for the guard rings. Nominally, no current will flow.
20	Ana. Ground	Power Supply	0.0 volts. Ground rail for the substrate contacts. Nominally, no current will flow.
21	AnaOut Left	Analog Out	Output from the left channel front end. Also connected to the left channel flash input. No special circuitry needed.
22	Vdd Cap	Power Supply	5.0 volts. The capacitor reset voltage. Attached to the cathode of all integrating capacitors. Must be quiet.
23	Ana. Power	Power Supply	5.0 volts. Power rail for Front End.

24	Ana. Ground	Power Supply	0.0 volts. Ground rail for substrate contact and Front End.
25	Input Left	Analog Input	Left channel input. Sits at 0.85 volts nominally. Connected by cable to PMT or strip chamber.
26	Dump Left	Analog Out	Left channel dump. Tied to 5.0 volt rail. Excess current from left channel passes through here.
27	Cas/Swt Current	Analog Input	Sets Cascode and Switch feedback amplifier currents. Not very critical. 3360 ohms to ground.
28	RcmpCurrent	Analog Input	Sets range comparator current level. Not very critical. 4000 ohms to ground.
29	VladTop	Ana. In/Out	Set internally to 4.0 volts by resistive divider. Can be overridden externally.
30	VladBot	Ana. In/Out	Set internally to 3.0 volts by resistive divider. Can be overridden externally.
32	Main Clamp	Analog Input	Passes through internal bipolar follower to set Main Clamp voltage. Nominally, 3.5 volts.
32	Top Clamp	Analog Input	Sets Top Clamp voltage. Nominally, 4.0 volts. VERY CRITICAL. VERY PROCESS DEPENDENT.
33	Splitter Bias	Analog Input	Sets the current through the Splitter and the Excess Current Splitter. Nominally, 95 kohm to ground.
34	Feedback Bias	Analog Input	Sets current through Splitter Feedback Amp and Excess Feedback amp. Not terribly critical. 127 ohm resistor to ground.
35	Dump Right	Analog Out	Right channel dump. Tied to 5.0 volt rail. Excess current from right channel passes through here.

36	Input Right	Analog Input	Right channel input. Sits at 0.85 volts nominally. Connected by cable to PMT or strip chamber.
37	Ana. Ground	Power Supply	0.0 volts. Ground rail for substrate contact and Front End.
38	Ana. Power	Power Supply	5.0 volts. Power rail for Front End.
39	VrefRCmp	Ana In/Out	The Range Comparator trip point. Nominally 3.2 volts, set internally by a resistive divider. Can be overridden.
40	AnaOut Right	Analog Out	Output from the right channel front end. Also connected to the right channel flash input. No special circuitry needed.
41	Ana. Ground	Power Supply	0.0 volts. Ground rail for the substrate contacts. Nominally, no current will flow.
42	Ana. Power	Power Supply	5.0 volts. Power rail for the guard rings. Nominally, no current will flow.
43	Flash Ground	Power Supply	0.0 volts. Ground rail for the 5 bit flash converter.
44	Flash Power	Power Supply	5.0 volts. Power rail for the 5 bit flash converter.
45	Dig. Ground	Power Supply	0.0 volts. Ground rail for the Level 1 FIFO and the Level 2 Buffer
46	Digital Power	Power Supply	5.0 volts. Power rail for Level1 FIFO and Level2 Buffer.
47	WB0_T	LVDS In	Least Significant Write Buffer Number. LVDS Levels. V(WB0_T) > V(WB0_B) is a Logical 1.
48	WB0_B	LVDS In	Least Significant Write Buffer Number. LVDS Levels. V(WB0_T) > V(WB0_B) is a Logical 1.

49	WB1_T	LVDS In	Most Significant Write Buffer Number. LVDS Levels. V(WB1_T) > V(WB1_B) is a Logical 1.
50	WB1_B	LVDS In	Most Significant Write Buffer Number. LVDS Levels. V(WB1_T) > V(WB1_B) is a Logical 1.
51	L1 Trigger_T	LVDS In	Level 1 Trigger input. LVDS levels. Active high trigger. V(L1_Trigger_T)> V(L1_Trigger_B) is a Logical 1.
52	L1 Trigger_B	LVDS In	Level 1 Trigger input. LVDS levels. Active high trigger. V(L1_Trigger_T)> V(L1_Trigger_B) is a Logical 1.
53	Reset_T	LVDS In	System reset input. Resets splitter only. LVDS levels. Active high reset. V(Reset_T)> V(Reset_B) is a Logical 1.
54	Reset_B	LVDS In	System reset input. Resets splitter only. LVDS levels. Active high reset. V(Reset_T)> V(Reset_B) is a Logical 1.
55	Clock_T	LVDS In	BCO clock input. LVDS levels. Rising edge of clock advances time slice. V(Clock_T)> V(Clock_B) is a Logical 1.
56	Clock_B	LVDS In	BCO clock input. LVDS levels. Rising edge of clock advances time slice. V(Clock_T)> V(Clock_B) is a Logical 1.
57	Mant0_B	LVDS Out	Least Significant Mantissa Bit. Connect through 100-ohm load to Mant0_T. V(Mant0_T)>V(Mant0_B) is a Logical 1
58	Mant0_T	LVDS Out	Least Significant Mantissa Bit. Connect through 100-ohm load to Mant0_B. V(Mant0_T)>V(Mant0_B) is a Logical 1
59	Mant1_B	LVDS Out	Middle Mantissa Bit. Connect through 100-ohm load to Mant1_T. V(Mant1_T)>V(Mant1_B) is a Logical 1

60	Mant1_T	LVDS Out	Middle Mantissa Bit. Connect through 100-ohm load to Mant1_B. V(Mant1_T)>V(Mant1_B) is a Logical 1
61	Mant2_B	LVDS Out	Middle Mantissa Bit. Connect through 100-ohm load to Mant2_T. V(Mant2_T)>V(Mant2_B) is a Logical 1
62	Mant2_T	LVDS Out	Middle Mantissa Bit. Connect through 100-ohm load to Mant2_B. V(Mant2_T)>V(Mant2_B) is a Logical 1
63	Mant3_B	LVDS Out	Middle Mantissa Bit. Connect through 100-ohm load to Mant3_T. V(Mant3_T)>V(Mant3_B) is a Logical 1
64	Mant3_T	LVDS Out	Middle Mantissa Bit. Connect through 100-ohm load to Mant3_B. V(Mant3_T)>V(Mant3_B) is a Logical 1
65	Pad Ground	Power Supply	0 volts. Must be able to sink 25 mA.
66	Pad Power	Power Supply	2.4 volts. Must be able to source 25 mA.
67	Mant4_B	LVDS Out	Most Significant Mantissa Bit. Connect through 100-ohm load to Mant4_T. V(Mant4_T)>V(Mant4_B) is a Logical 1
68	Mant4_T	LVDS Out	Most Significant Mantissa Bit. Connect through 100-ohm load to Mant4_B. V(Mant4_T)>V(Mant4_B) is a Logical 1
69	Range0_B	LVDS Out	Least Significant Range Bit. Connect through 100-ohm load to Range0_T. V(Range0_T)>V(Range0_B) is a Logical 1
70	Range0_T	LVDS Out	Least Significant Range Bit. Connect through 100-ohm load to Range0_B. V(Range0_T)>V(Range0_B) is a Logical 1
71	Range1_B	LVDS Out	Middle Range Bit. Connect through 100-ohm load to Range1_T.

			V(Range1_T)>V(Range1_B) is a Logical 1
72	Range1_T	LVDS Out	Middle Range Bit. Connect through 100-ohm load to Range1_B. V(Range1_T)>V(Range1_B) is a Logical 1
73	Range2_B	LVDS Out	Most Significant Range Bit. Connect through 100-ohm load to Range2_T. V(Range2_T)>V(Range2_B) is a Logical 1
74	Range2_T	LVDS Out	Most Significant Range Bit. Connect through 100-ohm load to Range2_B. V(Range2_T)>V(Range2_B) is a Logical 1
75	Pad Ground	Power Supply	0.0 Volts. Must be able to sink 25 mA.
76	Pad Power	Power Supply	2.4 Volts. Must be able to supply 25 mA.
77	Parity_B	LVDS Out	Even Parity Bit. Connect through 100-ohm load to Parity_T. V(Parity _T)> V(Parity _B) is a Logical 1
78	Parity_T	LVDS Out	Even Parity Bit. Connect through 100-ohm load to Parity_B. V(Parity _T)> V(Parity _B) is a Logical 1
79	CapID0_B	LVDS Out	Least Significant CapID Bit. Connect through 100-ohm load to CapID0_T. V(CapID0_T)>V(CapID0_B) is a Logical 1
80	CapID0_T	LVDS Out	Least Significant CapID Bit. Connect through 100-ohm load to CapID0_B. V(CapID0_T)>V(CapID0_B) is a Logical 1

LVDS stands for Low Voltage Differential Signaling. Signal_T is the “true” output, and Signal_B is the “invert” or “bar” output. V(Signal_T)>V(Signal_B) means “the voltage of the true version of the signal is greater than the voltage of the bar version of the signal”.

LVDS Levels are Vhi=1.4 volts and Vlo=1.0 volts. All LVDS inputs and output have diode ESD protection. The power supplies use grounded gate field effect transistors for ESD protection. The analog inputs and outputs have no appreciable ESD protection.

8 Alternate Pad Configuration

The two SMQIE chips will be placed on a card called a SQUID. The SQUID card is very small (12cm x 2.5cm) and densely packed. To facilitate this complicated design, it is necessary to bond half the SMQIE chips as “mirror images”. This is accomplished by

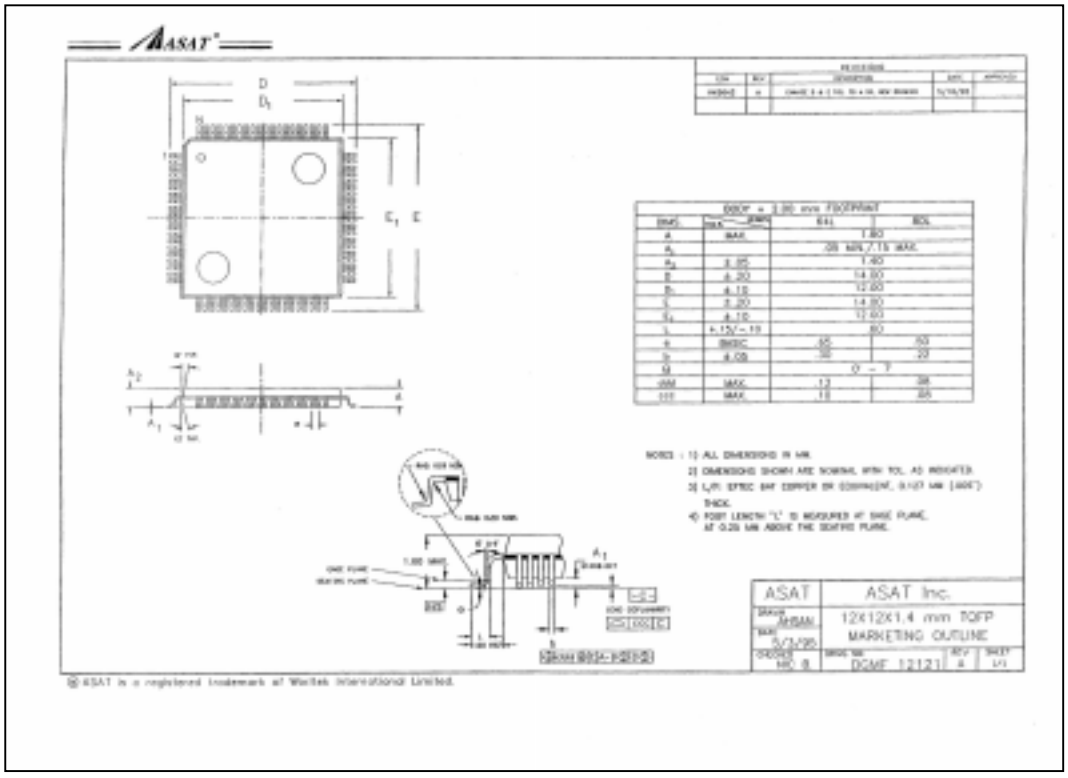

Figure 32 : Thin Quad-Flat Pack Specifications

ASAT, the company contracted to bond the SMQIE chips, by bonding half of the chips face up on the bottom of the package and the other half face down on the top of the package. The specifications for the packages are given above, the mirror image below.

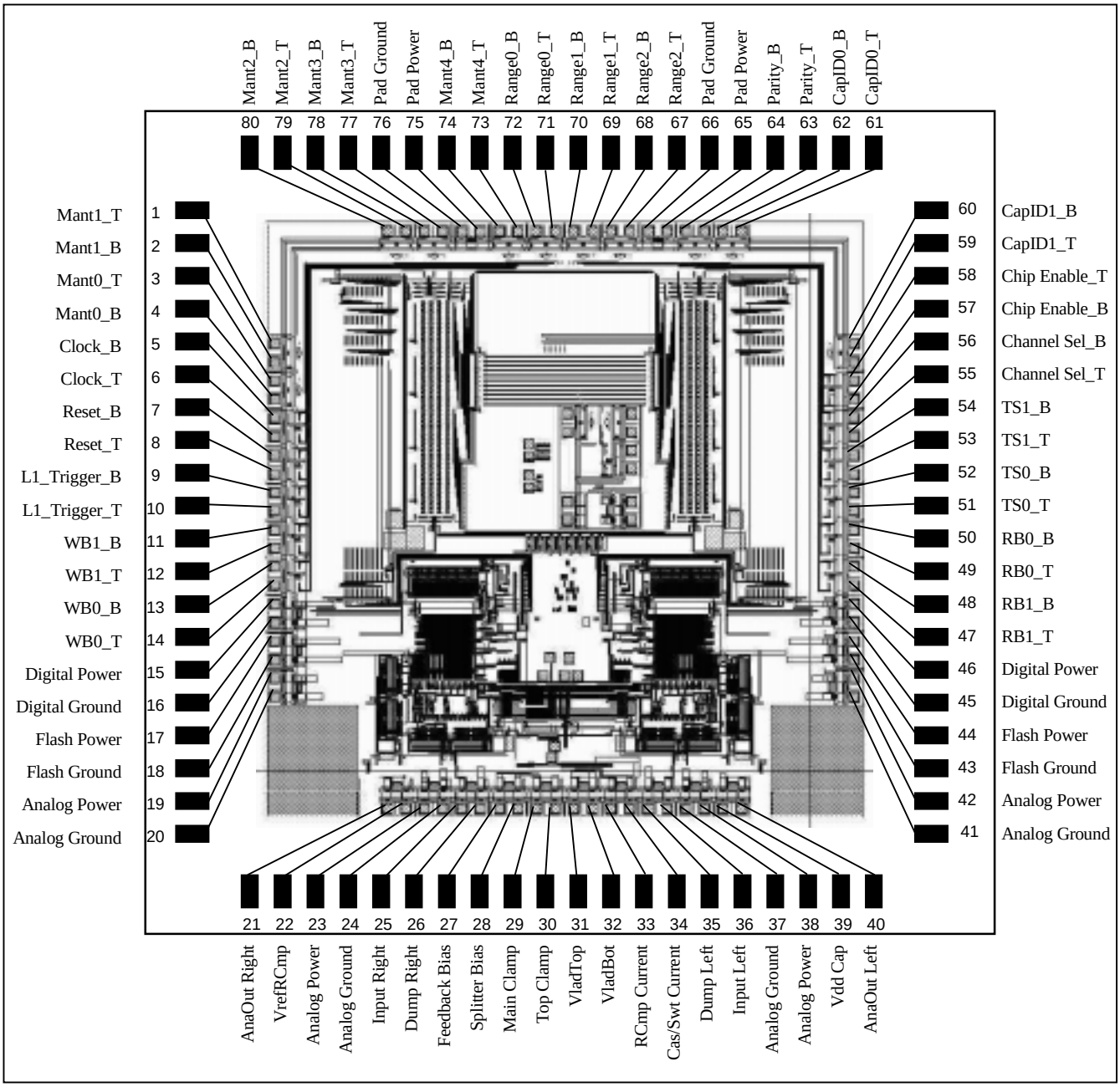

Figure 33: Alternate Pad Configuration

9 Simulations

9.1 Clock and Reset

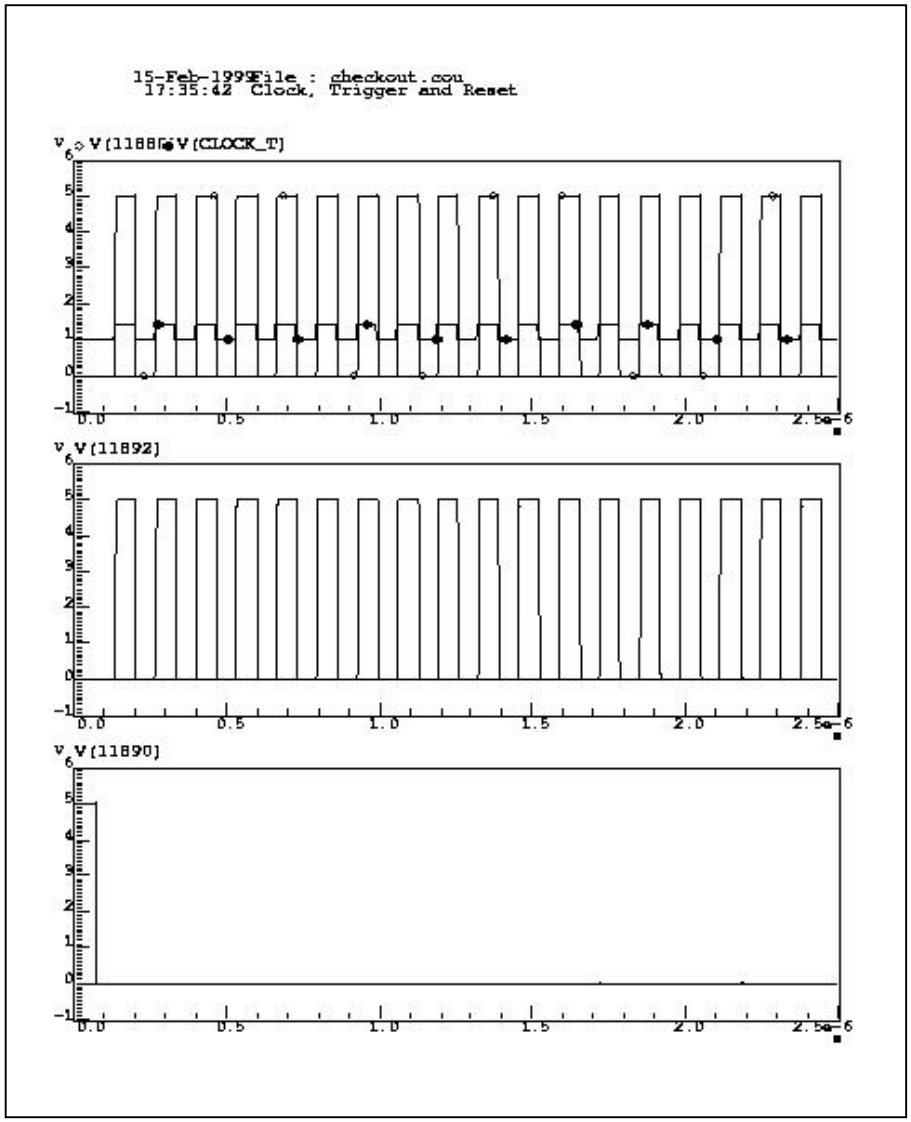

Figure 34: In the first frame is the LVDS Clock input shown with the CMOS internal clock. In the second frame, the CMOS internal trigger signal (The LVDS clock was used to generate it). In the third frame, the CMOS internal Reset signal. The figure shows that the LVDS receivers are working as expected.

9.2 Input and Analog Output

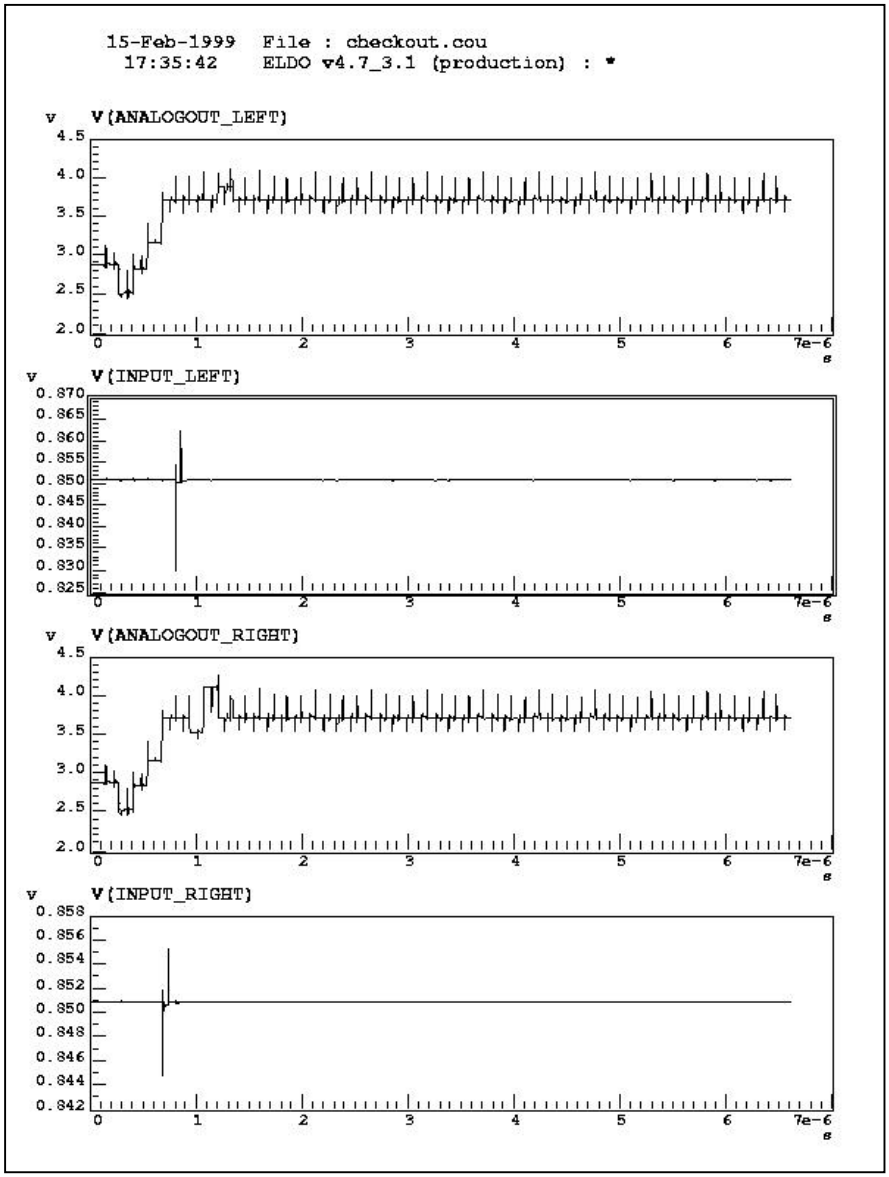

Figure 35: The top two panels show the left channel analog output and input. The bottom two panels show the right channel analog output and input. First, the output occurs two time slices after the input occurs. The right channel input was 2.5 pC. The left channel input was 10 pC. Imperfect biasing of the Top Clamp causes the analog output to go above pedestal

9.3 Cascode Voltage Regulation

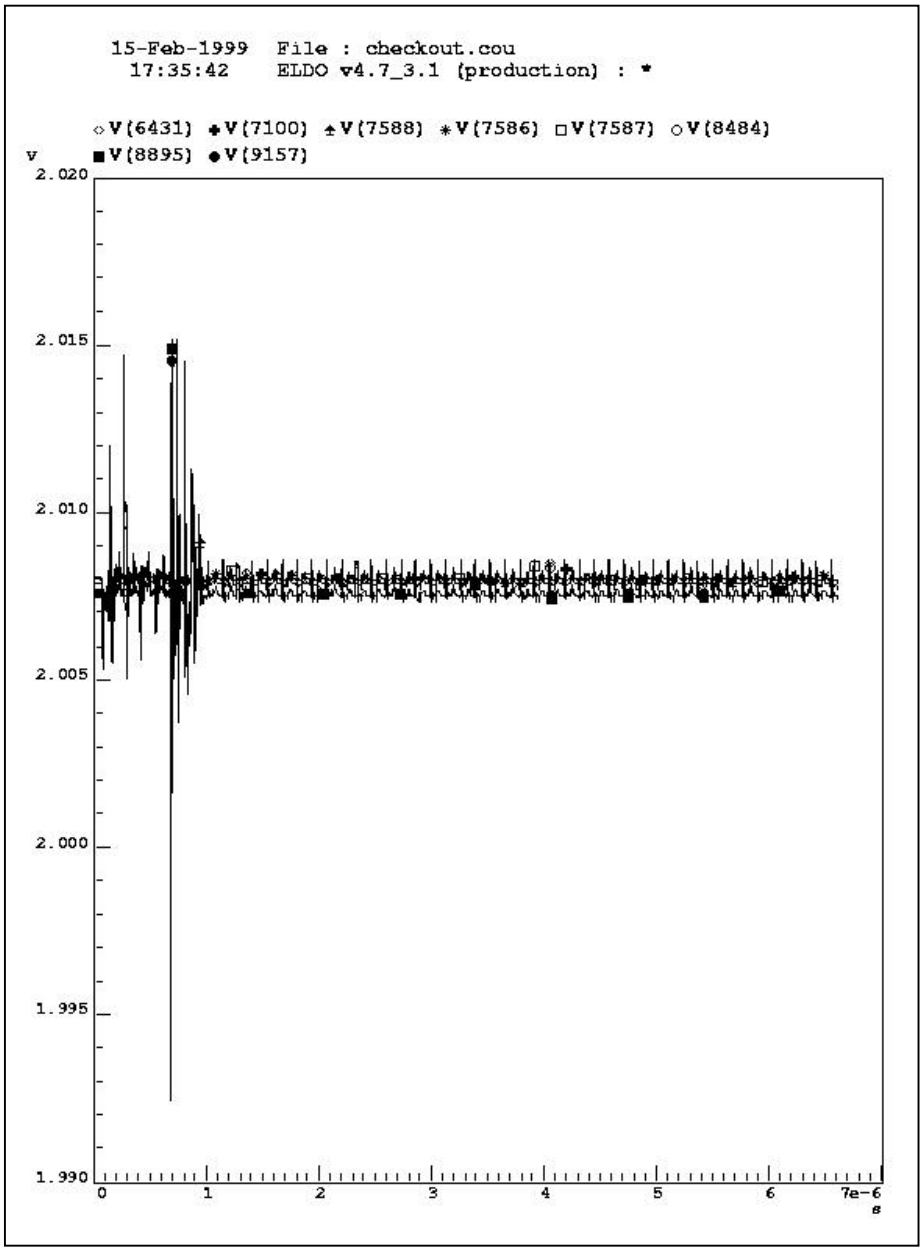

Figure 36: The cascode voltage regulation of the right channel is shown for all eight ranges. Note that in spite the fact that 2.5 pC should cause the I/2 and the I/4 range to dump, the Splitter Collectors are kept within 10 mV of their quiescent value of 2.0075 volts (2.0 volts nominally).

9.4 Switch Voltage Regulation

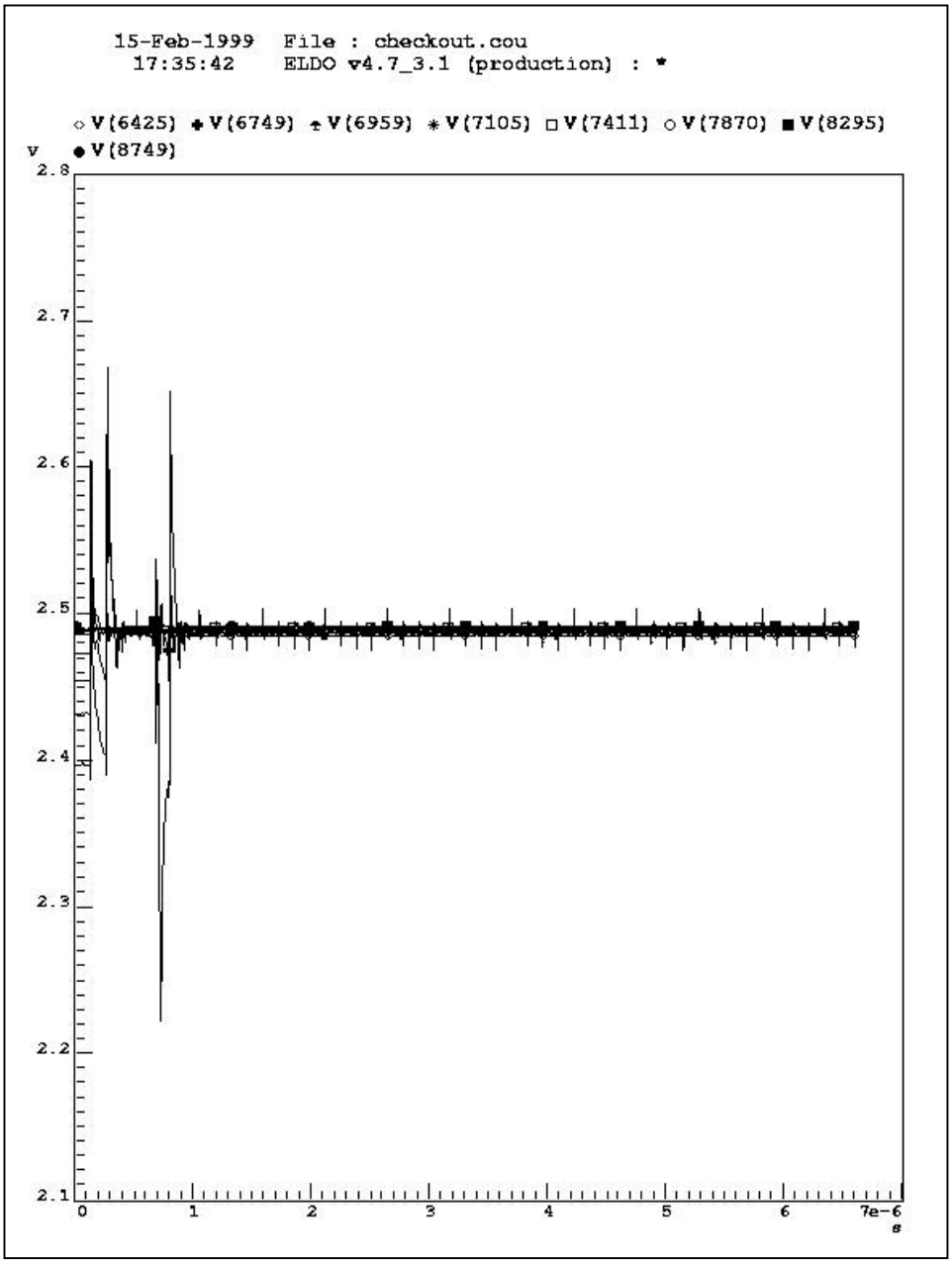

Figure 37: The Switch voltage regulation is also quite good. The only differences are that Range0 clearly dumps its excessive current. The improper biasing of the top clamp is seen here because the voltage at the input of the switch circuit cannot restore itself to its quiescent value before the beginning of the next time slice.

9.5 Internal Bias Levels

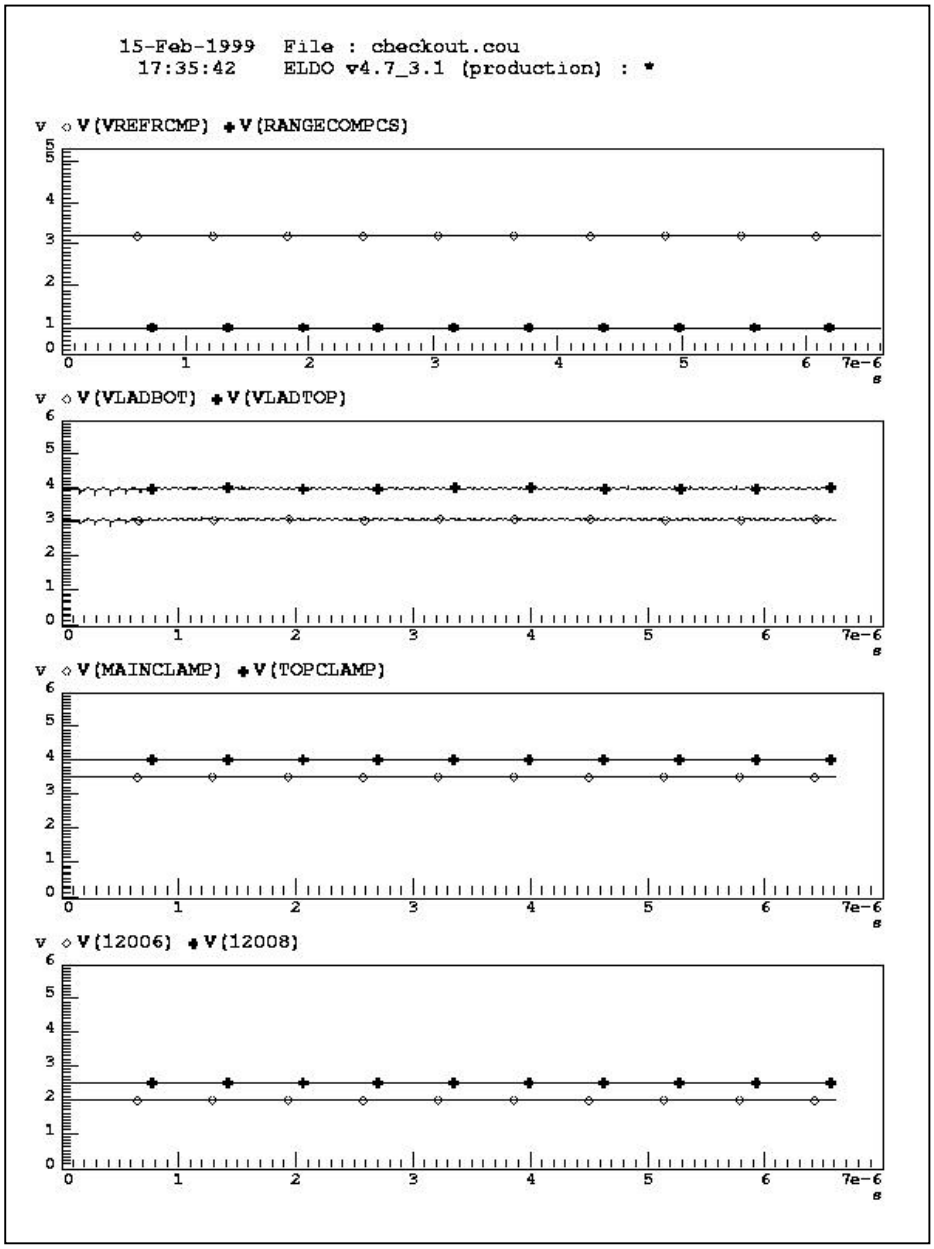

Figure 38: The first panel shows the trip point and the current source input to the range comparators. The second panels shows the top and bottom of the flash reference ladder at 4 and 3 volts. The third panel shows the clamps. The last panel shows the Switch and Cascode reference voltages at 2.5 and 2.0 volts, respectively

9.6 Pipeline Delay

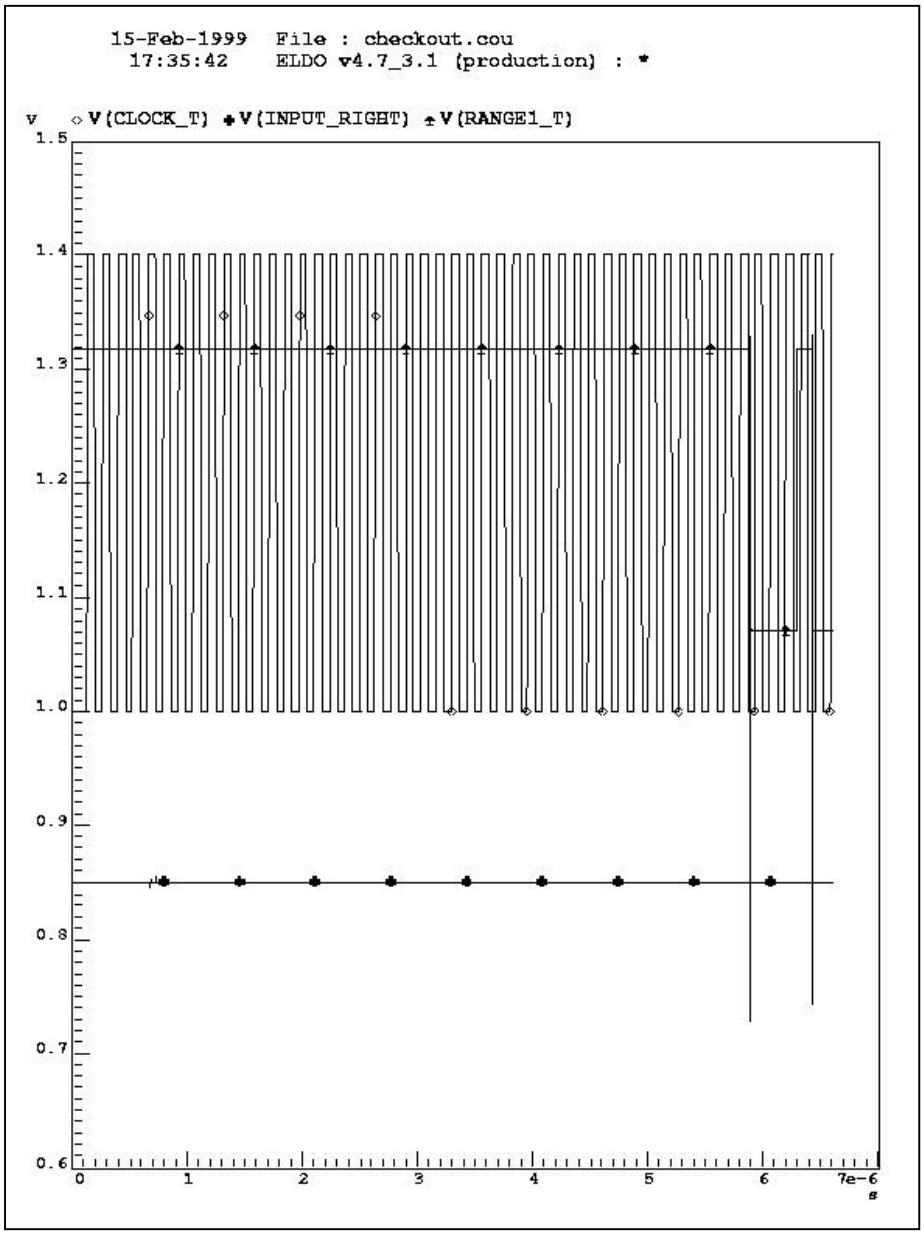

Figure 39: This figure shows the input voltage (quiescent value = 0.85 volts). At approximately 80ns, an event occurs. 42 time slices later, the results of that data come out of the LVDS outputs of the chip.